

ESP32-P4 Chip Revision v3.x

User Guide v1.0

Related Product:

ESP32-P4NRW16X

ESP32-P4NRW32X

PRELIMINARY



ESPRESSIF

About This Document

This document describes differences between chip revision v3.x and previous ESP32-P4 chip revisions.

Release Notes

Date	Version	Release Notes
2026.03	V1.0	First release.

Documentation Change Notification

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1. Design Changes in Chip Revision v3.x

Espressif has released ESP32-P4 chip revision v3.x that features wafer-level changes basing on previous ESP32-P4 chip revision v1.x. The design changes introduced on the ESP32-P4 chip revision v3.x are as below.

The following bugs are fixed. For details, please refer to [ESP32-P4 Series SoC Errata](#).

- [MSPI-749] Load Access Fault During Chip Power-on or Deep-Sleep Wake-up.
- [MSPI-750] PSRAM Unaligned DMA Read Operations May Return Old Data When Accessing Overlapping Addresses.
- [MSPI-751] Data Errors Caused by Asynchronous Timing Issues in the MSPI Address Overlap Detection Function When Read/Write Operations Overlap at Specific Frequencies.
- [ROM-764] Secure Boot Verification Failure Caused by Incorrect Buffer Address in ROM.
- [Analog-765] Output Regulators Cannot Generate a Reliable Supply When Peripheral Power Domain Is Off.
- [DMA-767] DMA Channel 0 Transaction ID Overlap Causes Permission Management Issue.
- [APM-560] Unauthorized AHB Access May Block Subsequent PSRAM or Flash Transactions.
- [ROM-770] Secure Download Mode Flash Power-On Failure.

The following modules are updated. For details, please refer to the specific chapter in [ESP32-P4 Technical Reference Manual](#).

1. High-Performance CPU

- Upgraded the HP system's dual-core RISC-V processor, increasing the max frequency from 360 MHz to 400 MHz.
- Fixed EXT_ILL_CSR bit 0 not updating for FPU Load/Store and FPU CSR instructions.
- Improved CLIC CSR access latency and compliance.
- Fixed bugs in trace, trigger, and HW loop logic.
- Improved dynamic clock-gating to reduce power consumption.
- Increased PMP entry count to 32.
- Added support for Bitwise-Manipulation extension (Zb).
- Improved PMP lock bit behavior.

- Added support for interrupt delegation to user mode.
- Added core mode and interrupt delegation status signals to interrupt matrix.
- Updated PIE for saturation and rounding.
- Added pad_cpu_wakeup_event input port to CPU.
- Changed HW loop counter width to 24 bits.

2. RISC-V Trace Encoder

- Added TRACE_CORE_WAITI bit in TRACE_DATA_REG to indicate whether the HP CPU cores are in WFI (wait-for-interrupt) state.

3. GDMA Controller

- Updated GDMA-AXI to support interrupt response during circular linked-list switching.
- Updated arbitration scheme to resolve false arbitration issues.
- Added error response logging for GDMA-AHB transfers, including address, channel ID, peripheral ID, and access type.
- Added clock gating for each GDMA-AHB channel, with a register option to force the clock on.
- Added support for INCR4/8/16 burst types; registers remain backward compatible.
- Added clarification that GDMA-AHB supports memory-to-memory data transfer only on channels 1 and 2.

4. 2D-DMA Controller

- Expanded PPA block size to 32×32 and widened related registers.
- Increased channel count to 4 TX and 3 RX.
- Updated reorder logic to support JPEG output conversion from YUV444/422 to YUV420.

5. System and Memory

- Changed cached region mapping to start from the bottom of L2MEM rather than the top.

6. IO MUX and GPIO Matrix

- Added IO hold during deep sleep for all IOs.
- Routed EMAC PPS signal to GPIO matrix.
- Routed parallel TX_CS signal to GPIO matrix.

7. Reset and Clock

- Added a new register HP_SYS_CLKRST_CPU_WAITI_CTRL0_REG.
- Added 160 MHz clock source to I2S.

8. Interrupt Matrix

- Enhanced Interrupt Matrix with interrupt remapping support, allowing user-mode delegated interrupts to be routed to the machine-mode interrupt port when the core runs in machine mode.
- Added core mode and delegate mode output signals from CPU to support remapping functionality.
- Added new peripheral interrupts.
- Added permission control to interrupt registers.

9. Low-power Management

- Added flash power quick discharge feature to enable faster ramp-up/down of the flash power supply, improving compatibility with a wider range of flash chips.
- Enabled wake-up via any interrupt when the TOP power domain remains powered during sleep; supported interrupts are configurable through a mask register located in the TOP domain.
- Added a power switch to fully power down the PUF memory.
- Optimized light sleep power consumption by adding a CPU power domain and updating memory retention modes.
- Enhanced power stability during Light-sleep using PVT monitoring to guard against power glitches.
- Removed debug probe port.

10. Permission Control

- Increased the number of configurable address ranges from 2 to 8 in PERI APM.
- Added permission control for TRNG.

11. Brown-out Detector

- Modified the voltage threshold.

12. AES Accelerator and External Memory Encryption and Decryption

- Added the pseudo-round function to enhance resistance against DPA attacks.

13. ECC Accelerator and ECDSA Digital Signature Peripheral

- Added P-384 curve support.

14. HMAC

- Added support for selecting key from key manager.

15. Key Manager

- Added support for HMAC and RSA_DS keys, and separated XTS keys into flash and PSRAM keys.

16. Random Number Generator

- Added separate RNG module.
- Added permission control bit for it in APM.

17. JPEG Codec

- Improved timing performance.
- Added one register to support extra color space.

18. Image Signal Processor

- Added BLC.
- Added DPC.
- Added WBG White Balance Gain.
- Updated AWB window (5 × 5 sub win).
- Added CROP.
- Updated CCM gain bit-width.
- Updated hue range from 0–255 to 0–359.
- Added shadow register.
- Enhanced the ISP CAM module to support HREF input functionality.
- Added RGB888-to-RGB565 and YUV422-to-YUV420 conversion before receiving pixel from MIPI CSI.
- Added 8-bit/16-bit byte swapping before receiving pixel from MIPI CSI.
- Added DMA flow control support in csi_bridge.

19. Pixel-Processing Accelerator

- Expanded SRM block size support up to 32 × 32.
- Added YUV422 and GRAY format support for SRM.
- Added YUV422/YUV420/GRAY support for BLEND input background and output.

20. LCD and Camera Controller

- Added byte swap support for CAM input.
- Updated CAM color mode conversion: removed YUV420 input support and changed conversion logic from RGB to YUV420.
- Increased LCD AFIFO depth to 32.

21. H264 Encoder

- Changed H264 core bitstream overflow status register into an interrupt source.
- Added support for multiple input color spaces in H264 core (also supported by H264 DMA).
- Added debug register.

22. I2S Controller

- Added 160 MHz clock source.

23. USB 2.0 OTG High-Speed

- Updated configuration to meet application requirements.

- Added description: up to 8 non-periodic transactions and 16 periodic transactions per microframe.

24.Parallel IO Controller

- Added a separate VALID/CS signal. The CS signal no longer controls data transmission.

25.Touch Sensor

- Modified the touch active detection method.
- Fixed the bug for updating baseline by software.

2. Impact on Customer Projects

This section is intended to help our customers to understand the impact of using chip revision v3.x in a new design or replacing older version SoC with chip revision v3.x in existing design.

2.1. Use Case 1: Hardware and Software Upgrade

1. Hardware Design Changes

For chip revisions v3.0 and later versions, the pin 54 is changed from NC to VDD_HP_1. A 1 MΩ resistor has been removed from the USB_DP pin. Two 499 kΩ resistors and one 22 pF capacitor are added in the DCDC circuit. For details, please refer to the latest [ESP32-P4 Hardware Design Guidelines](#).

2. Software Design Changes

When using ESP32-P4 chip revision v3.x, you must upgrade ESP-IDF to v5.5.3 or later, or v6.0 or later, and rebuild the firmware. These ESP-IDF versions introduce a new configuration option in sdkconfig:

[CONFIG_ESP32P4_SELECTS_REV_LESS_V3](#)

This option specifies which chip revision the compiled firmware targets:

- y: Targets v1.x chips
- n: Targets v3.x chips (default value)

If you previously developed your project using an intermediate ESP-IDF version, your project configuration may already contain:

```
CONFIG_ESP32P4_SELECTS_REV_LESS_V3=y
```

This setting will cause the firmware to either fail to download to a v3.x chip, or fail to boot properly after flashing. If you encounter this issue, manually change the option to:

```
CONFIG_ESP32P4_SELECTS_REV_LESS_V3=n
```

Then rebuild the firmware.

Chip revision v3.1 includes memory architecture adjustments and more than 50 hardware and register changes (including ISP, CPU, L2MEM, MSPI, security modules, etc.). Therefore, v1.x and v3.x chips cannot share the same firmware image. The target chip revision must be explicitly specified for compilation. If your product line includes both v1.x and v3.x chips, you must build separate firmware images for each revision.

3. Label Specification



Figure 3-1. The label of ESP32-P4NRW16X

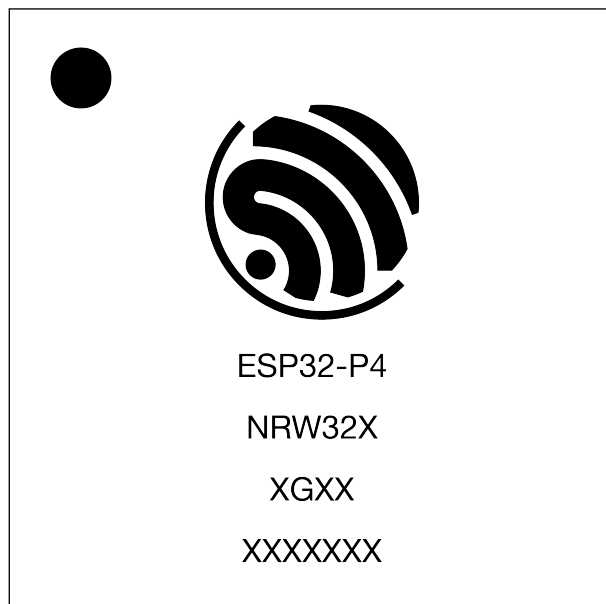


Figure 3-2. The label of ESP32-P4NRW32X

The figures above show the chip marking of chip revision v3.1: its manufacturing code is XGXX. For chip revision identification by chip marking, please refer to [ESP32-P4 Series SoC Errata](#).

4. Ordering Information

For product ordering, please refer to: [ESP Product Selector](#).

5. Related Documents

- [ESP32-P4 Datasheet](#)
- [ESP32-P4 Technical Reference Manual](#)
- [ESP32-P4 Hardware Design Guidelines](#)
- [ESP32-P4 Series SoC Errata](#)
- [ESP32-P4 Development Board User Guide](#)



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