ESP32-P4

Hardware Design Guidelines

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This document provides guidelines for the ESP32-P4 SoC.

Schematic Checklist	PCB Layout Design	Hardware Development

Chapter 1

Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32p4/index.html

1.1 About This Document

1.1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-P4 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif's standards. The guidelines are intended for hardware and application engineers.

1.1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32p4/index.html

1.2 Product Overview

ESP32-P4 is a system on a chip that integrates the following features:

- High-performance MCU with RISC-V 32-bit dual-core and single-core microprocessors
- Powerful image and voice processing capability
- 16 MB or 32 MB PSRAM in the chip's package
- 55 GPIOs, rich set of peripherals

Powered by 40 nm technology, ESP32-P4 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-P4 include:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics

- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Touch and Proximity Sensing

Note: Unless otherwise specified, "ESP32-P4" used in this document refers to the series of chips, instead of a specific chip variant.

1.3 Schematic Checklist

1.3.1 Overview

The integrated circuitry of ESP32-P4 series chips requires only 40 electrical components (resistors, capacitors, and inductors) and a crystal, as well as an SPI flash and a direct current to direct current converter (DCDC). This chapter details the schematic design of ESP32-P4.

The following figures show the reference schematics of ESP32-P4, which can be used as the basis of your schematic design.

Attention: For new designs, please refer to the schematic of chip revisions v3.0 and later versions.

Important: The main differences between chip revisions v1.0/v1.3 (**not recommended for new designs**) and v3.0 and later versions include the definition of pin 54, the 1 MΩ resistor on the DP pin, the two 499 kΩ resistors and one 22 pF capacitor in the DCDC circuit. For detailed descriptions of these differences, please refer to the following sections.

In chip revisions v3.0 and later versions, pin 54 of ESP32-P4 is defined as VDD_HP_1; in chip revisions v1.0 and v1.3, this pin is defined as NC.

Differences between ESP32-P4 chip revisions and how to distinguish them are described in ESP32-P4 Series SoC Errata.

Any basic ESP32-P4 circuit design includes the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash and PSRAM*
- *Clock source*
- *UART*
- *SPI*
- *Strapping pins*
- *GPIO*
- *ADC*

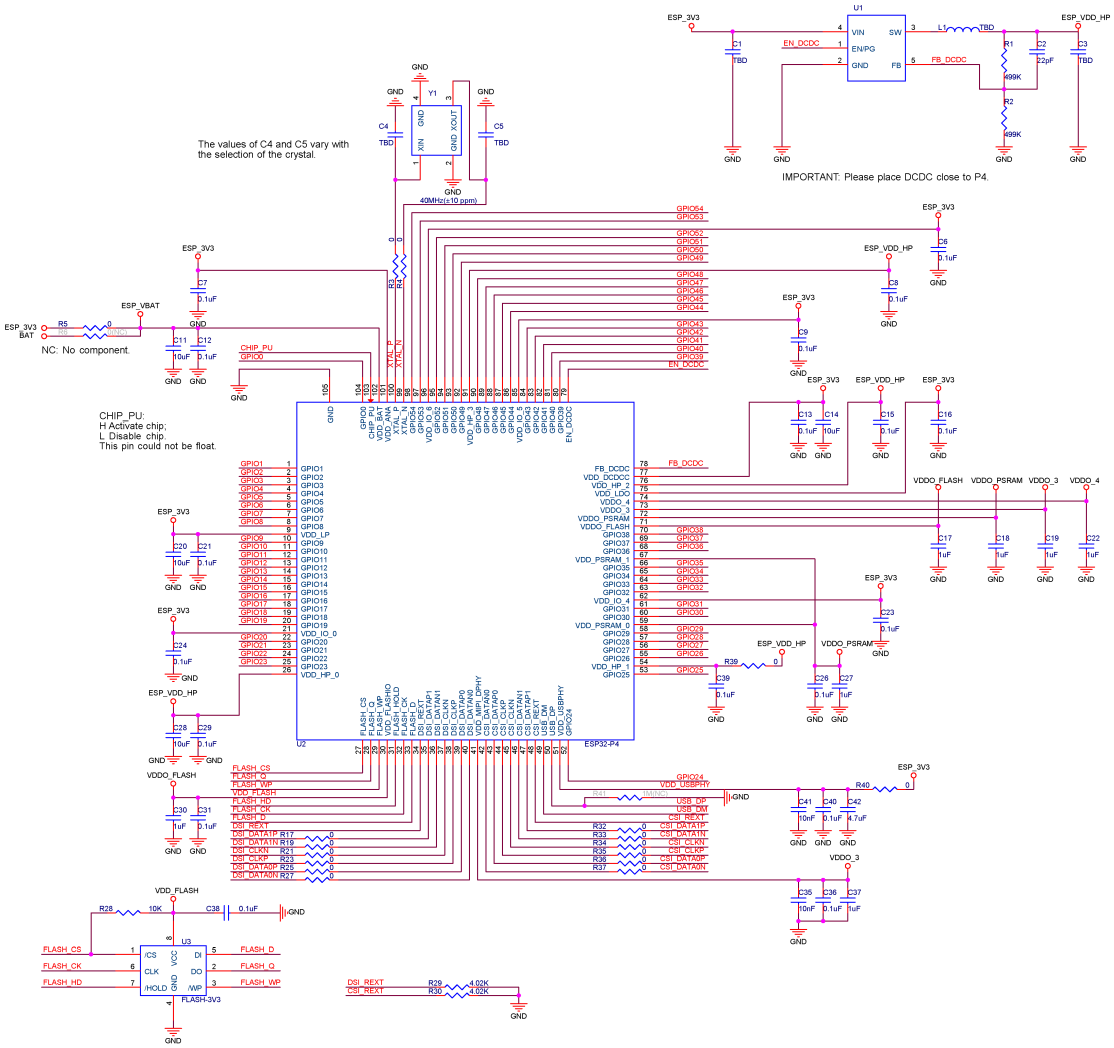

Fig. 1: ESP32-P4 Reference Schematic (Chip Revisions v3.0 and Later)

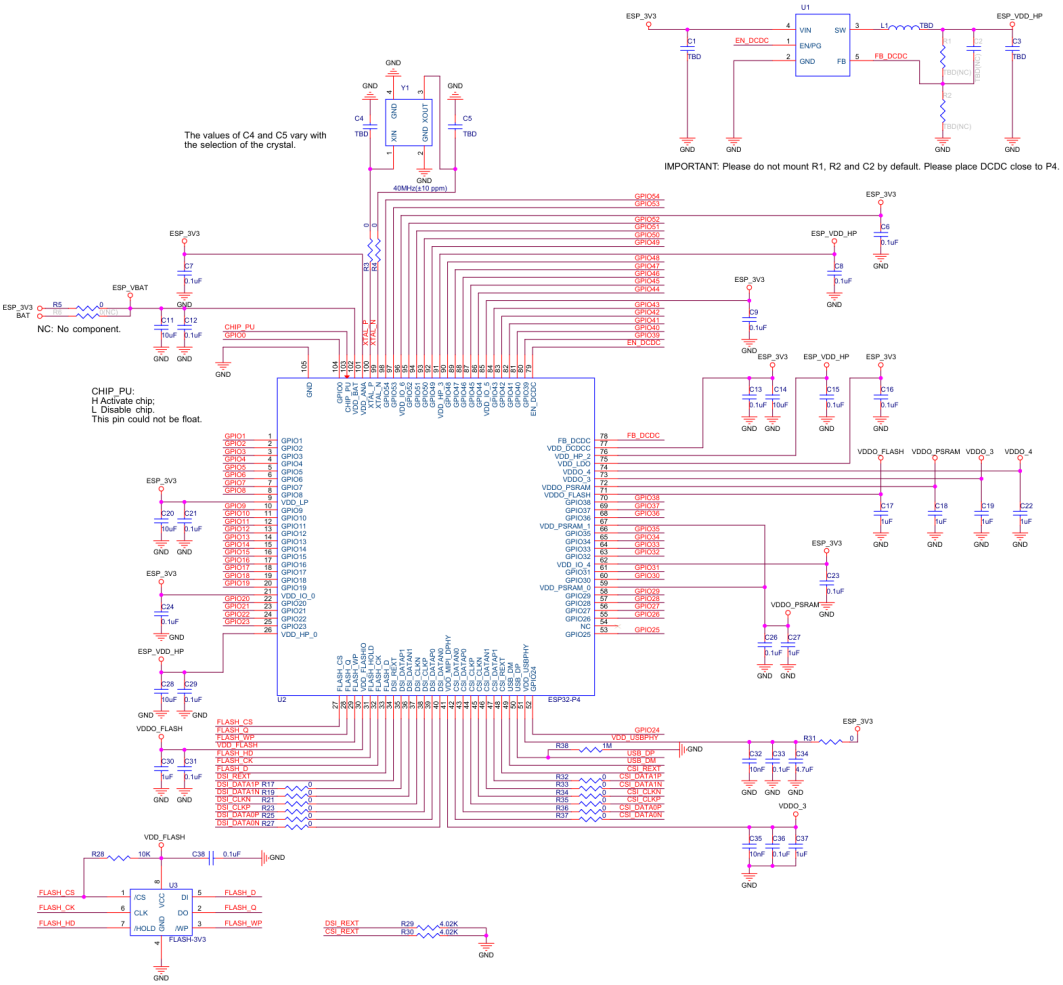

Fig. 2: ESP32-P4 Reference Schematic (Chip Revisions v1.0 and v1.3)

- *SDIO*
- *USB*
- *Touch sensor*
- *Ethernet MAC*
- *MIPI*

The rest of this chapter details the specifics of circuit design for each of these sections.

1.3.2 Power Supply

The general recommendations for power supply design are:

- For a single power supply, a voltage of 3.3 V is recommended.
- The minimum operating supply current of ESP32-P4 is 380 mA (including flash and PSRAM). For the supply current when peripherals are connected, please refer to *HP/LP IO Power Supply*, *MIPI PHY Power Supply* and *USB PHY Power Supply*. Calculate the required supply current based on your application and choose an appropriate power supply chip.
- It is suggested to add a 10 µF capacitor at each power entrance.
- The power scheme is as shown in Figure *ESP32-P4 Power Scheme*.

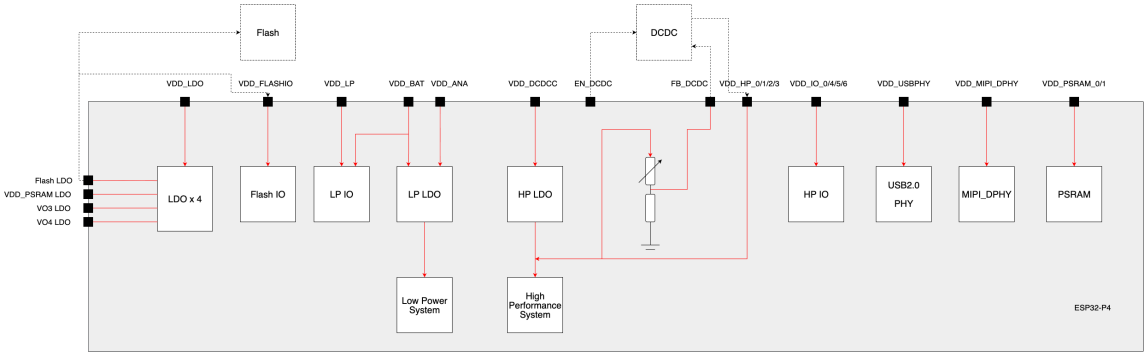

Fig. 3: ESP32-P4 Power Scheme

More information about power supply pins can be found in ESP32-P4 Series Datasheet > Section *Power Supply*.

HP/LP IO Power Supply

Pin No.	Pin Name	Direction	Voltage (V)	Max. Current (mA)	IO Pin	Capacitors (µF)
9	VDD_LP	Input	3.0 ~ 3.6	100	LP IO	0.1
21	VDD_IO_0	Input	1.65 ~ 3.6	100	HP IO	0.1
62	VDD_IO_4	Input	1.65 ~ 3.6	100	HP IO	0.1
85	VDD_IO_5[1]	Input	1.65 ~ 3.6	100	HP IO	0.1
96	VDD_IO_6	Input	1.65 ~ 3.6	100	HP IO	0.1

[1] If VDD_IO_5 is used as the IO power supply for SD 3.0 interface, please refer to *SDIO* for the circuit reference.

MIPI PHY Power Supply

The VDD_MIPI_DPHY of ESP32-P4 is the power supply pin for MIPI PHY. The operating voltage range is 2.25 V ~ 2.75 V. The maximum current consumption is 50 mA. It is recommended to use the internal voltage regulator for power supply, and place 10 nF + 0.1 µF + 1 µF capacitors near VDD_MIPI_DPHY in the circuit.

If the MIPI function is not required, VDD_MIPI_DPHY can be left floating.

> **Attention:** The voltage level of MIPI signals is defined by the MIPI specification. For details, please refer to the relevant MIPI protocol documentation. Note that this is a different concept from the MIPI DPHY voltage level. The 1.8 V/3.3 V levels mentioned in Camera/Display Datasheet refer to signals other than the MIPI signals (Data Lane & CLK), such as MCLK and I2C. The voltage level of MIPI signals is handled internally by the ESP32-P4' s built-in MIPI DPHY and requires no additional configuration.

USB PHY Power Supply

The VDD_USBPHY of ESP32-P4 is the power supply pin for USB PHY. The operating voltage range is 2.97 V ~ 3.63 V. The maximum current consumption is 20 mA. It is recommended to place 10 nF + 0.1 µF + 4.7 µF capacitors near VDD_USBPHY in the circuit.

If DP and DM are not required, the VDD_USBPHY power supply can be left floating.

If DP and DM are required, for chip revisions v1.0 and v1.3 (**not recommended for new designs**), note that the VDD_USBPHY power supply exhibits leakage current in low power modes. Therefore, it is recommended to add a MOSFET circuit to completely shut off this power supply in low power modes. During the validation phase, a 0 Ω series resistor can be added on VDD_USBPHY.

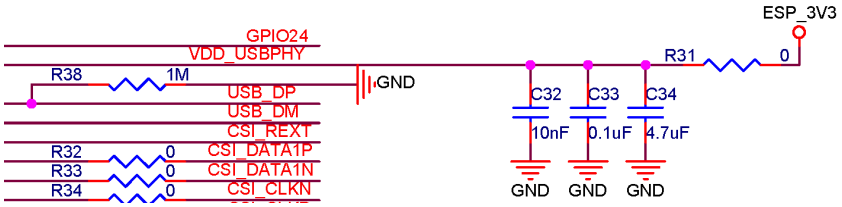

Fig. 4: VDD_USBPHY Reference Schematic (Chip Revisions v1.0 and v1.3)

In chip revisions v3.0 and later versions, this issue has been fixed, and the 0 Ω series resistor can be retained for design compatibility.

Flash and PSRAM IO Power Supply

The VDD_FLASHIO of ESP32-P4 is the power supply pin for FLASH IO. The operating voltage is 1.65 V ~ 3.6 V. This power is supplied by VDDO_FLASH from the voltage regulator. It is recommended to place 0.1 µF + 1 µF capacitors near VDD_FLASHIO in the circuit.

VDD_PSRAM_0 and VDD_PSRAM_1 are power supply pins for PSRAM IO. The operating voltage is 1.65 V ~ 1.95 V. This power is supplied by VDDO_PSRAM from the voltage regulators. It is recommended to place 0.1 µF + 1 µF capacitors near VDD_PSRAM_0 and VDD_PSRAM_1 in the circuit.

Analog Power Supply

The VDD_ANA of ESP32-P4 is an analog power supply pin. The operating voltage range is 3.0 V ~ 3.6 V. It is recommended to place a 0.1 µF capacitor near VDD_ANA in the circuit. The VDD_BAT is also an analog power supply pin. The operating voltage range is 2.5 V ~ 3.6 V. It is recommended to place 0.1 µF + 10 µF capacitors near VDD_BAT.

Pin VDD_BAT must not be left floating. An external battery can be connected. For details, refer to the ESP32-P4 Battery Backup Solution.

Digital Power Supply

VDD_HP_0, VDD_HP_1, VDD_HP_2, and VDD_HP_3 of the ESP32-P4 are digital power supply pins, working in a voltage range of 0.99 V ~ 1.3 V. This power is supplied by ESP_VDD_HP from the external DCDC. It is recommended to place a 10 µF capacitor at the main power source and 0.1 µF capacitors near each power pin.

Internal Voltage Regulators and External DCDC

The VDD_LDO of ESP32-P4 provides power for the low dropout regulators (LDOs). The operating voltage ranges from 3.0 V to 3.6 V. VDD_DCDCC provides power for DCDC. The operating voltage ranges from 3.0 V to 3.6 V. Due to the high current on these pins, place a 10 µF capacitor on the power traces of VDD_LDO and VDD_DCDCC, and add a 0.1 µF capacitor at each pin.

The LDO outputs VDDO_FLASH to power the external flash. The default output is 3.3 V, but it can be configured to 1.8 V by programming EFUSE_0PXA_TIEH_SEL_0.

Note: When using a 1.8 V SPI flash, it is recommended to disconnect the power connection between VDDO_FLASH and the SPI flash until the VDDO_FLASH output voltage has been correctly configured to 1.8 V, to prevent damage to the 1.8 V flash caused by excessive supply voltage.

If this solution is intended for mass production, please contact sales for further support.

Table 1: VDDO_FLASH Voltage

Power	EFUSE_0PXA_TIEH_SEL_0	Voltage
flash LDO	0	3.3 V
	2	1.8 V

The LDO outputs VDDO_PSRAM to power the in-package PSRAM. The typical output voltage is 1.9V, which requires software configuration. The default output is 0.

The LDO outputs VDDO_3/4 to power the peripherals. The maximum output current is 50 mA. The output voltage ranges from 0.5V to 2.7V/3.3V, which also requires software configuration. The default output is 0.

For software configuration, please refer to Low Dropout Linear Regulator (LDO).

It is recommended to place a 1 µF capacitor near the VDDO_FLASH, VDDO_PSRAM, and VDDO_3/4 in the circuit.

The VDD_HP_0/1/2/3 is powered by an external DC-DC converter (DCDC), with the following details:

- The input of the external DCDC is the same as the VDD_DCDCC power supply.
- EN_DCDC is the enable pin of the external DCDC. In download mode or when there is no firmware, the voltage on EN_DCDC is 0. After the firmware starts normally, EN_DCDC is controlled internally. In download mode, the EN_DCDC voltage remains at 0. In sleep mode, this pin can be used to disable the power supply to reduce power consumption.
- FB_DCDC is the feedback pin of the external DCDC.
- EN_DCDC and FB_DCDC pins are fully controlled by the internal circuitry of ESP32-P4 by default. Ensure that they are connected to the EN and FB pins of the external DCDC, respectively, and that the DCDC regulator is placed close to the ESP32-P4. When designing the layout for chip revisions v1.0 and v1.3 (**not recommended for new designs**), you must reserve pad locations for the feedback resistor and feedback capacitor (components not required). For chip revisions v3.0 and later versions, the feedback resistor and the feedback capacitor must be populated.

Please use verified DCDC models: ETA3485, SY8088, RY3420, BL8028, LP3219, or TLV62569. The input/output specifications and inductor parameters should follow the respective datasheets. Below is the circuit design for TLV62569.

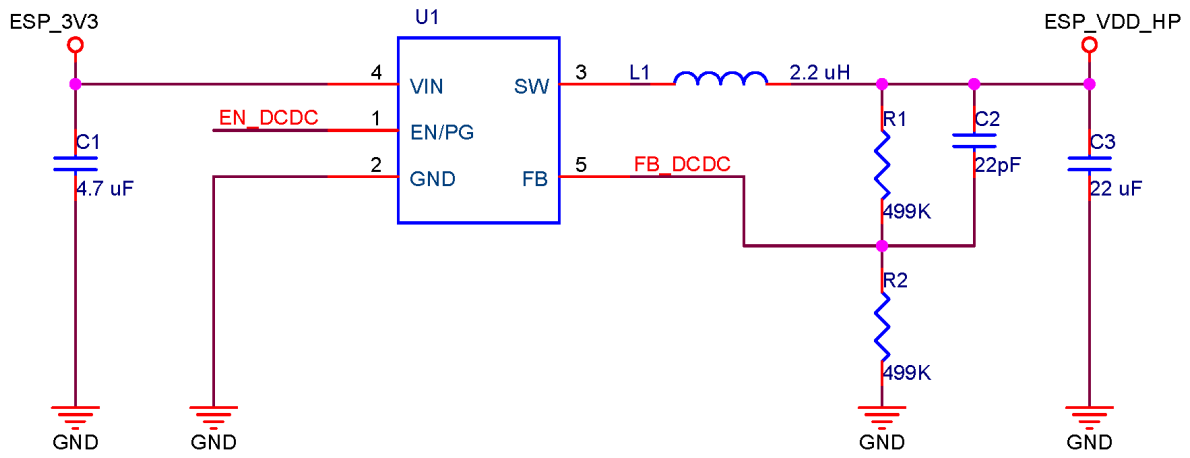

Fig. 5: TLV62569 Schematic (Chip Revisions v3.0 and Later)

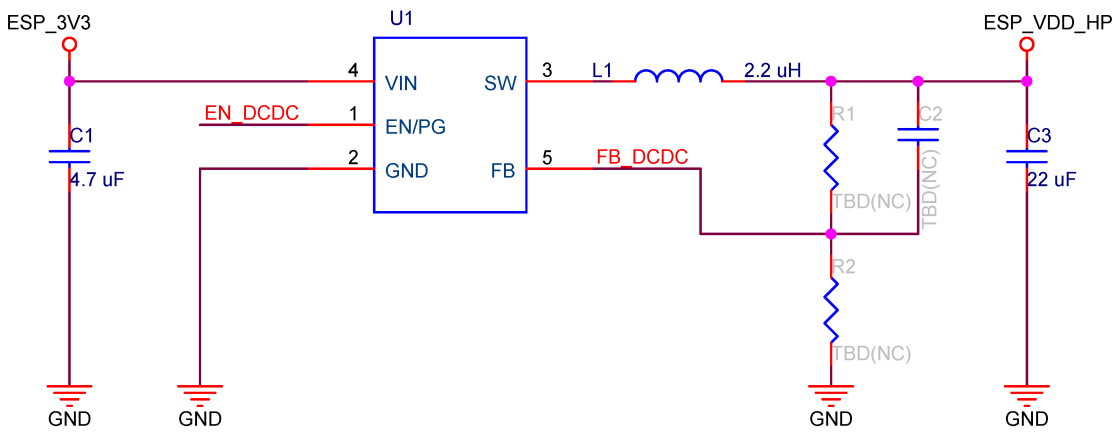

Fig. 6: TLV62569 Schematic (Chip Revisions v1.0 and v1.3)

1.3.3 Chip Power-up and Reset Timing

ESP32-P4' s CHIP_PU pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-P4 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of (–0.3 ~ 0.25 × VDD_BAT) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

Figure *ESP32-P4 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-P4.

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

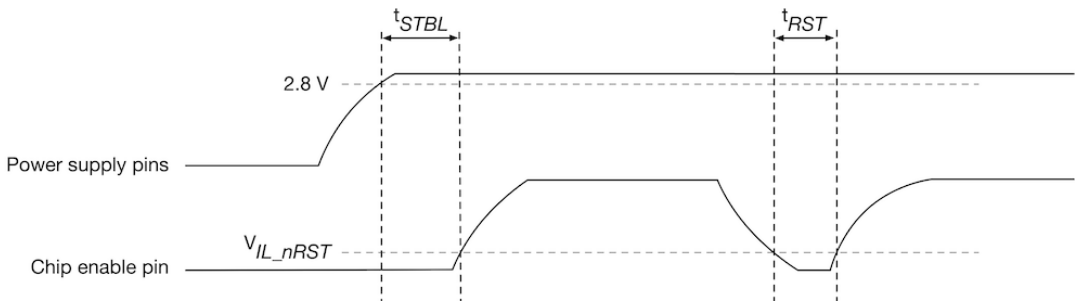

Fig. 7: ESP32-P4 Power-up and Reset Timing

Table 2: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (µs)
t_{STBL}	Time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	1000

Attention:

- CHIP_PU must not be left floating.
- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 µF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
  - Slow power rise or fall, such as during battery charging.
  - Frequent power on/off operations.
  - Unstable power supply, such as in photovoltaic power generation.

  Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:
  - Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
  - Implementing reset functionality through a button or the main controller.

1.3.4 Flash and PSRAM

ESP32-P4 requires off-package flash for storing application firmware and data. ESP32-P4 supports up to 64 MB flash, which can be connected via SPI, Dual SPI, and Quad SPI.

ESP32-P4 includes OPI/HPI 1.8 V PSRAM, which is not pinned out externally.

The following table lists the pin mapping between ESP32-P4 and off-package flash for Quad SPI mode. Please note that the pins can connect to one flash at the maximum.

Table 3: Mapping of chip and package to Quad SPI Flash pins

ESP32-P4	External Package Flash (Quad SPI)
FLASH_CK	CLK
FLASH_CS	CS#
FLASH_D	DI
FLASH_Q	DO
FLASH_WP	WP#
FLASH_HOLD	HOLD#

By default, VDDO_FLASH is used as the power supply for flash, and VDDO_PSRAM is used as the power supply for PSRAM.

When VDDO_FLASH is in the output mode of 3.3 V, consider the impact of R_{VFB} on VDD_LDO. For example, when connecting a 3.3 V flash, the following condition must be met:

$$VDD_LDO > VDD_flash_min + I_flash_max \times R_{VFB}$$

In the formula above, VDD_flash_min is the minimum operating voltage of the flash, I_flash_max is the maximum operating current of the flash, and R_{VFB} is the on-resistance in 3.3 V mode.

Attention:

- It is recommended to add zero-ohm resistor footprints in series on the SPI communication lines. These footprints provide flexibility for future adjustments, such as tuning drive strength, mitigating RF interference, correcting signal timing, and reducing noise, if needed.
- Place a pull-up resistor at the FLASH_CS pin.
- It is recommended to place a 0.1 µF capacitor at the flash power supply pin.

1.3.5 Clock Source

ESP32-P4 supports two external clock sources:

- *External crystal clock source (Compulsory)*
- *RTC clock source (Optional)*

External Crystal Clock Source (Compulsory)

The ESP32-P4 firmware only supports 40 MHz crystal.

The circuit for the crystal is shown in Figure *ESP32-P4 Schematic for External Crystal*. Note that the accuracy of the selected crystal should be within ±10 ppm.

The initial values of external capacitors C4 and C5 can be determined according to the formula:

$$C_L = \frac{C4 \times C5}{C4 + C5} + C_{stray}$$

In the formula above, the value of C_L (load capacitance) can be found in the crystal' s datasheet, and the value of C_{stray} refers to the PCB' s stray capacitance. The values of C4 and C5 need to be further adjusted after an overall test.

RTC Clock Source (Optional)

ESP32-P4 supports an external 32.768 kHz crystal to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

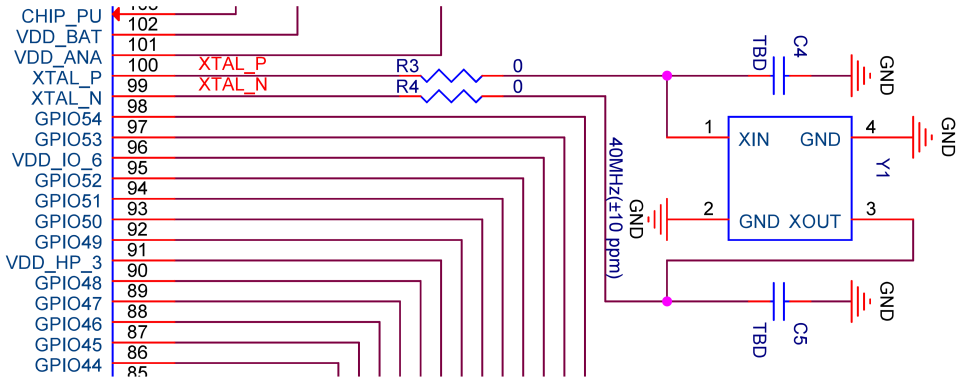

Fig. 8: ESP32-P4 Schematic for External Crystal

Figure *ESP32-P4 Schematic for 32.768 kHz Crystal* shows the schematic for the external 32.768 kHz crystal.

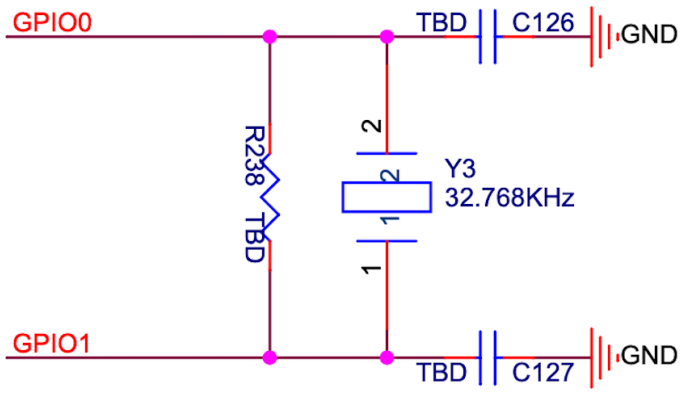

Fig. 9: ESP32-P4 Schematic for 32.768 kHz Crystal

Please note the requirements for the 32.768 kHz crystal:

- Equivalent series resistance (ESR) ≤ 70 kΩ.
- Load capacitance at both ends should be configured according to the crystal' s specification.

The parallel resistor R is used for biasing the crystal circuit (5 MΩ < R ≤ 10 MΩ). In general, you do not need to populate the resistor.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

1.3.6 UART

ESP32-P4 includes five UART interfaces, UART0 ~ UART4, all of which support both hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF). In addition, ESP32-P4 includes one LP UART interface, which also supports both hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF).

The UART0_TXD pin is GPIO37, and the UART0_RXD pin is GPIO38. The other UART0 signals can be mapped to any available GPIO through software configurations. The LP UART TXD is LP GPIO14, and the LP UART RXD is LP GPIO15. The other LP UART signals can be mapped to any available GPIO through software configurations.

Typically, UART0 is used for download and log printing. For instructions on how to download via UART0, please refer to Section *Download Guidelines*.

It is recommended to use UART1 ~ UART4 as communication serial ports.

1.3.7 SPI

When using the SPI function, to improve EMC performance, add a series resistor (or ferrite bead) and a capacitor to ground on the SPI_CLK trace. If space allows, it is recommended to also add a series resistor and capacitor to ground on other SPI traces. Ensure that the RC/LC components are placed close to the pins of the chip or module.

1.3.8 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

GPIO34, GPIO35, GPIO36, GPIO37, and GPIO38 are strapping pins.

All the information about strapping pins is covered in ESP32-P4 Series Datasheet > Section *Boot Configurations*. In this document, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO35, GPIO36, GPIO37, and GPIO38 controls the boot mode. See Table *Chip Boot Mode Control*.

Table 4: Chip Boot Mode Control

Boot Mode	GPIO35	GPIO36	GPIO37	GPIO38
SPI Boot Mode (Default)	1	Any value	Any value	Any value
Joint Download Mode[2]	0	1	Any value	Any value

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure *Setup and Hold Times for Strapping Pins* and Table *Description of Timing Parameters for Strapping Pins*.

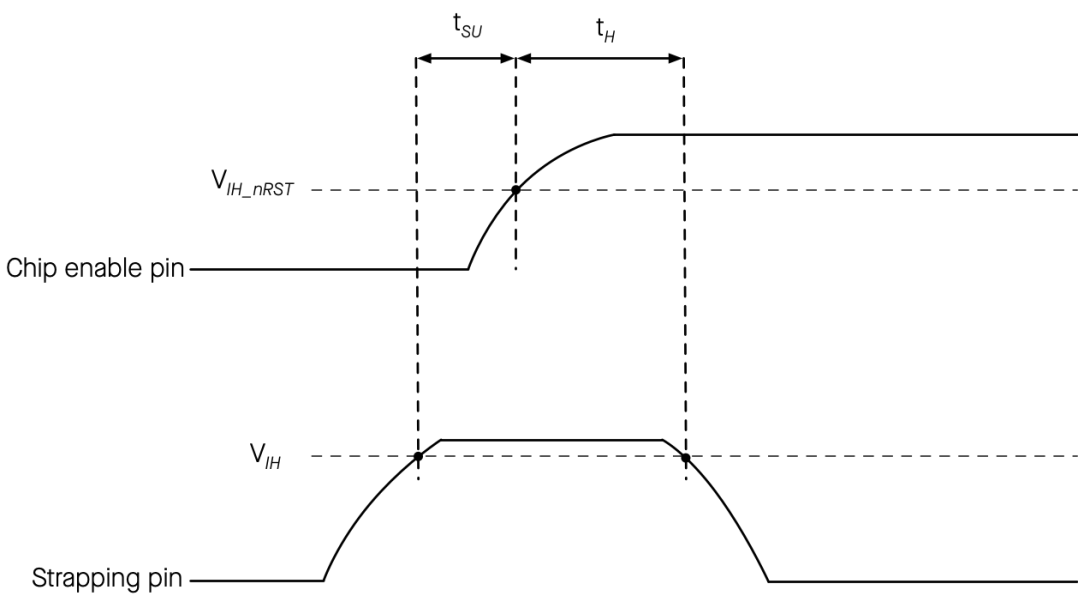

Fig. 10: Setup and Hold Times for Strapping Pins

[2] The following download methods are supported under Joint Download Mode:
- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB 2.0 OTG Download Boot
- UART Download Boot
- SPI Slave Download Boot

Table 5: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_PU) is pulled high to activate the chip.	0
t_H	Time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

Attention:

- It is recommended to reserve a pull-up resistor at the GPIO35.
- Do not add high-value capacitors at GPIO35, otherwise, the chip may enter Joint Download mode instead of SPI Boot mode.

1.3.9 GPIO

The pins of ESP32-P4 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations (see ESP32-P4 Series Datasheet > Appendix *ESP32-P4 Consolidated Pin Overview*), whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP32-P4 Technical Reference Manual > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP32-P4 Series Datasheet > Section *Peripherals*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.
- Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in Table *IO MUX Pin Functions*. It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- Only GPIOs in the VDD_LP power domain can be controlled in Deep-sleep mode.
- When powered solely by the battery, only GPIOs in the VDD_BAT power domain can be controlled.

Table 6: IO MUX Pin Functions

Pin Number	Pin Name	Power Supply Pin	At Reset	After Reset
1	GPIO1	VDD_LP/VDD_BAT	–	–
2	GPIO2	VDD_LP/VDD_BAT	–	IE, WPU
3	GPIO3	VDD_LP/VDD_BAT	–	IE
4	GPIO4	VDD_LP	–	IE
5	GPIO5	VDD_LP	–	–
6	GPIO6	VDD_LP	–	–
7	GPIO7	VDD_LP	–	–
8	GPIO8	VDD_LP	–	–
10	GPIO9	VDD_LP	–	–
11	GPIO10	VDD_LP	–	–
12	GPIO11	VDD_LP	–	–
13	GPIO12	VDD_LP	–	–
14	GPIO13	VDD_LP	–	–
15	GPIO14	VDD_LP	–	–
16	GPIO15	VDD_LP	–	–
17	GPIO16	VDD_IO_0	–	–

continues on next page

Table 6 – continued from previous page

Pin Number	Pin Name	Power Supply Pin	At Reset	After Reset
18	GPIO17	VDD_IO_0	–	–
19	GPIO18	VDD_IO_0	–	–
20	GPIO19	VDD_IO_0	–	–
22	GPIO20	VDD_IO_0	–	–
23	GPIO21	VDD_IO_0	–	–
24	GPIO22	VDD_IO_0	–	–
25	GPIO23	VDD_IO_0	–	–
52	GPIO24	VDD_IO_4	–	–
53	GPIO25	VDD_IO_4	–	IE, USB_PU
55	GPIO26	VDD_IO_4	–	–
56	GPIO27	VDD_IO_4	–	–
57	GPIO28	VDD_IO_4	–	–
58	GPIO29	VDD_IO_4	–	–
60	GPIO30	VDD_IO_4	–	–
61	GPIO31	VDD_IO_4	–	–
63	GPIO32	VDD_IO_4	IE	–
64	GPIO33	VDD_IO_4	IE	–
65	GPIO34	VDD_IO_4	IE	–
66	GPIO35	VDD_IO_4	IE, WPU	–
68	GPIO36	VDD_IO_4	IE	–
69	GPIO37	VDD_IO_4	IE	–
70	GPIO38	VDD_IO_4	IE	–
80	GPIO39	VDD_IO_5	–	–
81	GPIO40	VDD_IO_5	–	–
82	GPIO41	VDD_IO_5	–	–
83	GPIO42	VDD_IO_5	–	–
84	GPIO43	VDD_IO_5	–	–
86	GPIO44	VDD_IO_5	–	–
87	GPIO45	VDD_IO_5	–	–
88	GPIO46	VDD_IO_5	–	–
89	GPIO47	VDD_IO_5	–	–
90	GPIO48	VDD_IO_5	–	–
92	GPIO49	VDD_IO_6	–	–
93	GPIO50	VDD_IO_6	–	–
94	GPIO51	VDD_IO_6	–	–
95	GPIO52	VDD_IO_6	–	–
97	GPIO53	VDD_IO_6	–	–
98	GPIO54	VDD_IO_6	–	–
104	GPIO0	VDD_LP/VDD_BAT	–	–

1.3.10 ADC

When using the ADC function, place a 0.1 µF capacitor to ground near the pin to improve accuracy.

ADC Channel Signal	Pin Name
ADC1_CHANNEL0	GPIO16
ADC1_CHANNEL1	GPIO17
ADC1_CHANNEL2	GPIO18
ADC1_CHANNEL3	GPIO19
ADC1_CHANNEL4	GPIO20
ADC1_CHANNEL5	GPIO21
ADC1_CHANNEL6	GPIO22
ADC1_CHANNEL7	GPIO23
ADC2_CHANNEL0	GPIO49
ADC2_CHANNEL1	GPIO50
ADC2_CHANNEL2	GPIO51
ADC2_CHANNEL3	GPIO52
ADC2_CHANNEL4	GPIO53
ADC2_CHANNEL5	GPIO54

1.3.11 SDIO

ESP32-P4 series chips integrate an SD/MMC host controller, which cannot operate as a slave. The SD/MMC host peripheral provides two slots. Each slot can be used independently to connect to an SD card, SDIO device, or eMMC chip.

Slot 1 (SDMMC_HOST_SLOT_0) signals are fixed to the GPIO pins listed in the table below via the IO MUX and are dedicated to UHS-I mode.

Table 7: Slot 1 (SDMMC_HOST_SLOT_0) Signal Mapping

Signal	Pin Name
SD1_CDATA0_PAD	GPIO39
SD1_CDATA1_PAD	GPIO40
SD1_CDATA2_PAD	GPIO41
SD1_CDATA3_PAD	GPIO42
SD1_CCLK_PAD	GPIO43
SD1_CCMD_PAD	GPIO44
SD1_CDATA4_PAD	GPIO45
SD1_CDATA5_PAD	GPIO46
SD1_CDATA6_PAD	GPIO47
SD1_CDATA7_PAD	GPIO48

Slot 2 (SDMMC_HOST_SLOT_1) signals can be routed to any GPIO pins through the GPIO matrix, making this slot suitable for non–UHS-I applications.

Please add a pull-up resistor to each SDIO GPIO pin and reserve a series resistor on each SDIO signal line. In addition, reserve a capacitor to ground on the SDIO CLK line for signal tuning.

SDIO 3.0 protocol specifies that the voltage of SDIO GPIOs should switch automatically. Therefore, it is recommended to connect the SDIO GPIO power domain VDD_IO_5 and the external pull-up power supply to VDDO_4. The SD card' s power supply should be connected to the 3.3 V power supply of the system.

To reduce the power consumption of the SD card and reset it, you can populate a MOSFET at the power supply circuit of SD card and control it via GPIO.

1.3.12 USB

ESP32-P4 integrates a USB serial/JTAG controller that uses GPIO24 and GPIO25 as USB D- and USB D+ by default.

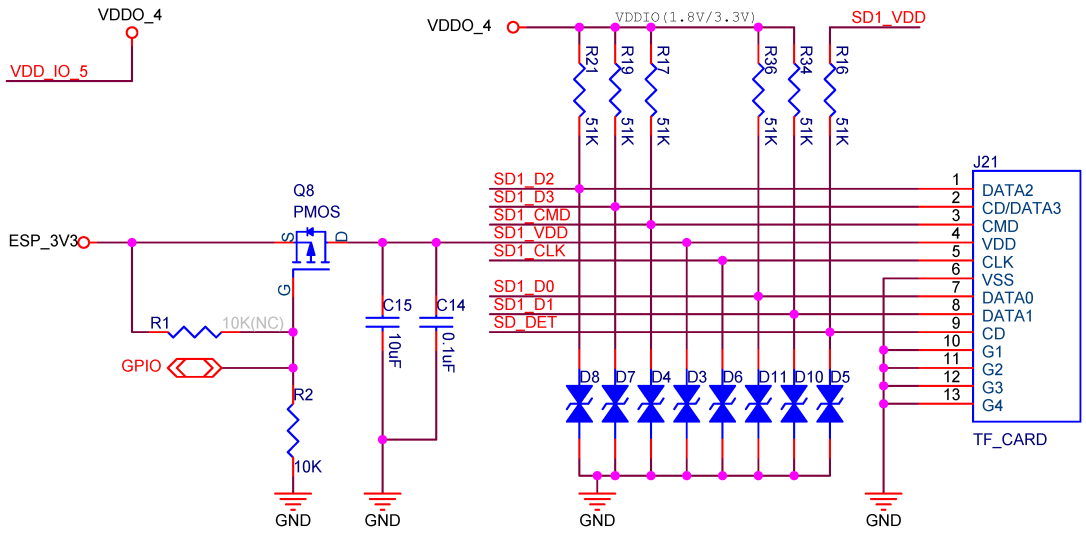

Fig. 11: ESP32-P4 SD 3.0 Card Power Circuit

ESP32-P4 also features a USB 2.0 Full-Speed OTG peripheral with an integrated transceiver. By default, the USB 2.0 Full-Speed OTG uses GPIO26 and GPIO27 as USB D- and USB D+.

When using the USB serial/JTAG controller and USB 2.0 Full-Speed OTG, please note the following:

- The roles of the USB D- and USB D+ pins can be swapped.
- If only one function is in use, you can select either GPIO24/GPIO25 or GPIO26/GPIO27.
- If both functions are used simultaneously, GPIO24/GPIO25 and GPIO26/GPIO27 will serve as two separate pins for each function.

ESP32-P4 also features a USB 2.0 High-Speed OTG peripheral with an integrated transceiver, where DM and DP respectively serve as the USB D- and USB D+.

When using chip revisions v1.0 and v1.3 (**not recommended for new designs**), add a 1 MΩ pull-down resistor on the DP pin to reduce the large transient current on VDD_USBPHY when CHIP_PU is pulled low.

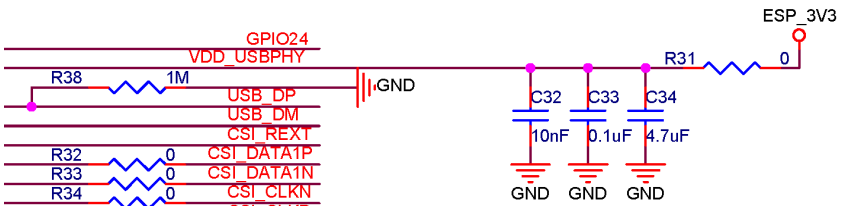

Fig. 12: DP Pull-down Resistor (Chip Revisions v1.0 and v1.3)

In chip revisions v3.0 and later versions, this issue has been fixed, allowing the retention of a 1 MΩ pull-down resistor for design compatibility.

It is recommended to add a 22/33 Ω series resistor and optional ground capacitors on the D- and D+ lines of the USB 2.0 Full-Speed OTG. These components should be placed close to the chip end.

At the USB connector end, it is advisable to include ESD protection diodes. When using the USB 2.0 High-Speed OTG peripheral, the parasitic capacitance of the diode should not exceed 1 pF to avoid poor signal quality and unstable transmission.

ESP32-P4 also supports downloading via USB. For details, please refer to *Download Guidelines*.

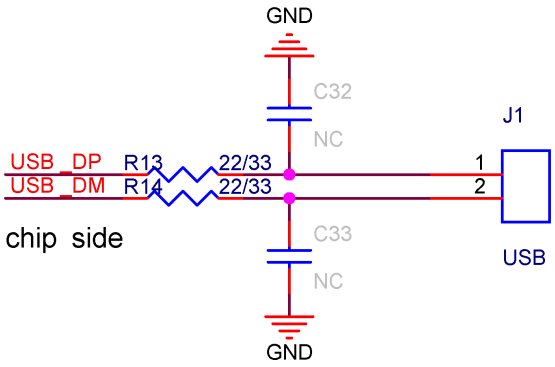

Fig. 13: ESP32-P4 USB RC Circuit

1.3.13 Touch Sensor

ESP32-P4 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected.

The touch sensing performance can be further enhanced by the waterproof design, detection of frequency hopping, and digital filtering feature.

Table 8: Touch Sensor Functions

GPIO Pin Name	Touch Sensor Function
GPIO2	TOUCH_CHANNEL1
GPIO3	TOUCH_CHANNEL2
GPIO4	TOUCH_CHANNEL3
GPIO5	TOUCH_CHANNEL4
GPIO6	TOUCH_CHANNEL5
GPIO7	TOUCH_CHANNEL6
GPIO8	TOUCH_CHANNEL7
GPIO9	TOUCH_CHANNEL8
GPIO10	TOUCH_CHANNEL9
GPIO11	TOUCH_CHANNEL10
GPIO12	TOUCH_CHANNEL11
GPIO13	TOUCH_CHANNEL12
GPIO14	TOUCH_CHANNEL13
GPIO15	TOUCH_CHANNEL14

When using the touch function, it is recommended to populate a series resistor at ESP32-P4 side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value depends on the actual test results of the product.

1.3.14 Ethernet MAC

Refer to the table below for the GPIO configuration of the EMAC RMII interface.

Table 9: EMAC Interface Configuration

Signal	Pin Name
RMII_CRSDV	GPIO28, GPIO45, GPIO51
RMII_RXD0	GPIO29, GPIO46, GPIO52
RMII_RXD1	GPIO30, GPIO47, GPIO53
RMII_RXER	GPIO31, GPIO48, GPIO54
RMII_CLK	GPIO32, GPIO44, GPIO50
RMII_TXEN	GPIO33, GPIO40, GPIO49
RMII_TXD0	GPIO34, GPIO41
RMII_TXD1	GPIO35, GPIO42
RMII_TXER	GPIO36, GPIO43

It is recommended to populate a series resistor on the RMII CLK line.

Please note that the clock signal in the RMII interface is input-only. If you need a clock output solution, please use the REF_50M_CLK_PAD signal (GPIO23/GPIO39).

1.3.15 MIPI

ESP32-P4 includes an MIPI DSI interface for connecting displays with an MIPI interface, and an MIPI CSI interface for connecting cameras with an MIPI interface. Please populate a 4.02 kΩ pull-down resistor to both the CSI_REXT pin and DSI_REXT pin.

It is recommended to reserve series resistors on the MIPI communication lines (initially 0 Ω). The main purposes are to reduce drive current, adjust timing, and improve interference resistance.

If an RF module is included in the design, please also add series resistors on the CSI interface at the device end to minimize interference with the RF module.

Attention:

- If the MIPI interface is not used, the power and external resistor pins can be left floating.
- For MIPI interface devices, please use GPIO for control signals.

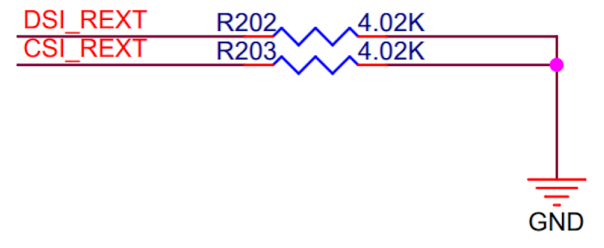

Fig. 14: ESP32-P4 Schematic for MIPI Signal

1.4 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-P4 PCB layout using an ESP32-P4 development board as an example.

Considering the communication quality of high-speed signal lines and potential interference with the RF module, please use at least a four-layer PCB design, as follows:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): Route power traces here. If possible, route high-speed signal traces here and ensure a complete reference plane.
- Layer 4 (BOTTOM): Route some signal traces here.

1.4.1 Power Supply

- Whenever possible, route the power traces on the inner layers (not the ground layer) and connect them to the chip pins through vias. Ensure the power traces are surrounded by ground copper.
- The trace width for the 3.3 V main power supply should be at least 25 mil.
- For the power traces of VDD_LP, VDD_IO_0, VDD_IO_4, VDD_IO_5, VDD_IO_6, VDD_BAT and VDD_ANA, use a trace width of at least 10 mil. Place a 10 µF capacitor at the power entry point for this series of power supply and a 0.1 µF capacitor for each power pin.
- The trace width for the main power supply traces of VDD_HP_0, VDD_HP_1, VDD_HP_2, and VDD_HP_3 should be at least 20 mil. Place a 10 µF capacitor at the power entry point for this series of power supply and a 0.1 µF capacitor for each power pin.
- For VDD_LDO and VDD_DCDCC, which handle higher current, use a trace width of at least 20 mil and place a 10 µF capacitor close to each power pin.
- It is recommended to use a star routing method to distribute power traces to each power pin.
- Because the VDD_HP power supply is by default fully controlled internally by ESP32-P4, the external DCDC should be placed close to the chip to ensure that the input, output, and feedback loops are as short as possible.

1.4.2 Crystal

Figure *ESP32-P4 Crystal Layout* shows a reference PCB layout of crystal design.

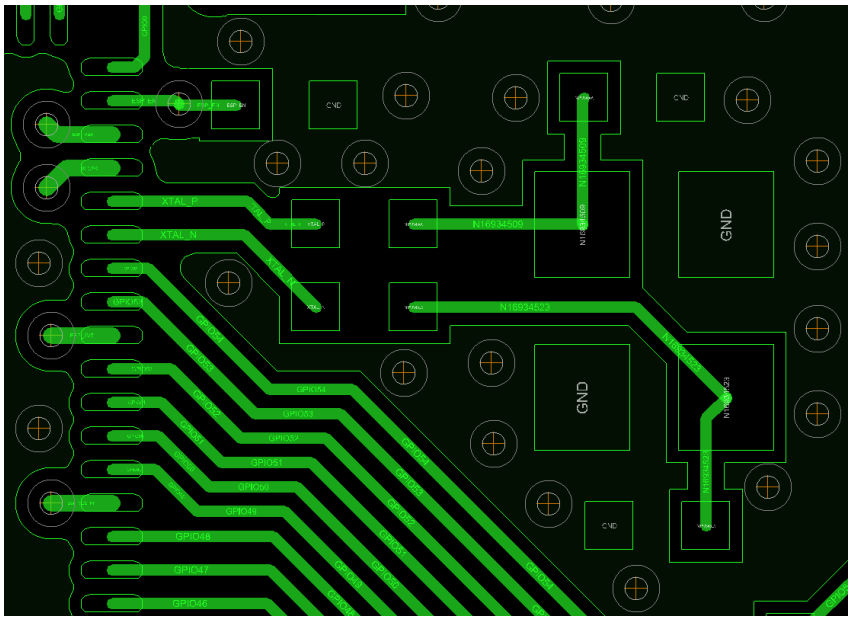

Fig. 15: ESP32-P4 Crystal Layout

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the crystal and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 4.5 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces.

- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is recommended not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by ground copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a complete large-area ground plane around the crystal.

1.4.3 USB

The USB layout should meet the following guidelines:

- Reserve space for resistors and capacitors on the USB traces close to ESP32-P4.
- Use differential pairs with a differential impedance of 90 Ω with a tolerance of ±10%. Use differential pairs and route them in parallel at equal lengths.
- USB differential traces should minimize via transitions as much as possible to ensure better impedance control and avoid signal reflections. If vias are necessary, add a pair of ground return vias at each transition point.
- Ensure there is a continuous reference layer (a ground layer is recommended) beneath the USB traces.
- Surround the USB traces with ground copper.

1.4.4 SDIO

The SDIO layout should follow the guidelines below:

- Minimize parasitic capacitance of SDIO traces as they involve high-speed signals.
- The trace lengths for SDIO_CMD and SDIO_DATA0 ~ SDIO_DATA3 should be within ±50 mil of the SDIO_CLK trace length. Use serpentine routing if necessary.
- For SDIO routing, maintain a 50 Ω single-ended impedance with a tolerance of ±10%.
- Keep the total trace length from SDIO GPIOs to the master SDIO interface as short as possible, ideally within 2000 mil.
- Ensure that SDIO traces do not cross layers. Besides, a reference plane (preferably a ground plane) must be placed beneath the traces, and continuity of the reference plane must be ensured.
- It is recommended to surround the SDIO_CLK trace with ground copper.
- For multi-layer PCB designs, it is recommended to route SDIO traces to an inner layer through vias immediately after being drawn out from the chip. This helps minimize interference with high-speed signal lines. Add a pair of ground return vias at each via transition point.

1.4.5 Touch Sensor

ESP32-P4 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip' s internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure *ESP32-P4 Typical Touch Sensor Application* depicts a typical touch sensor application.

To prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

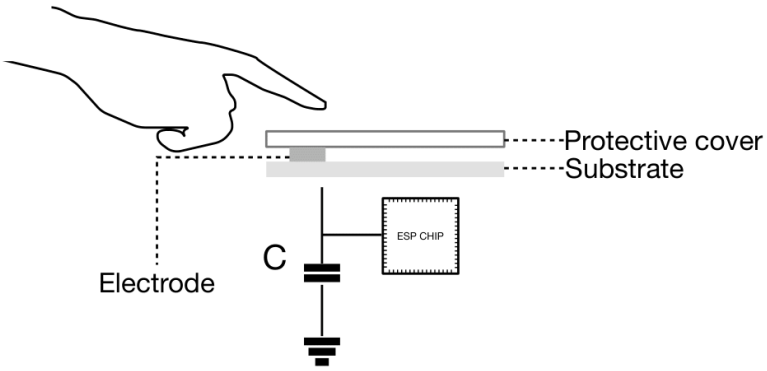

Fig. 16: ESP32-P4 Typical Touch Sensor Application

Figure *ESP32-P4 Electrode Pattern Requirements* shows the proper and improper size or shape of electrode. Please note that the examples illustrated in the figure are not of actual scale. It is suggested to use a human fingertip as reference.

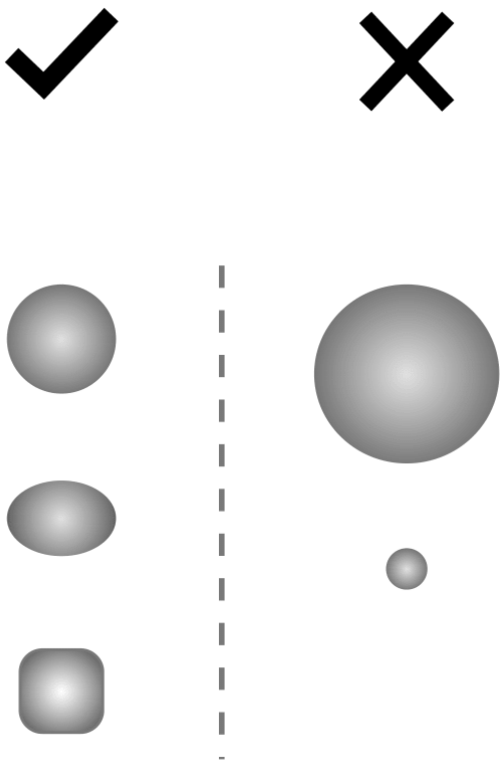

Fig. 17: ESP32-P4 Electrode Pattern Requirements

PCB Layout

Figure *ESP32-P4 Sensor Track Routing Requirements* illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.

- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

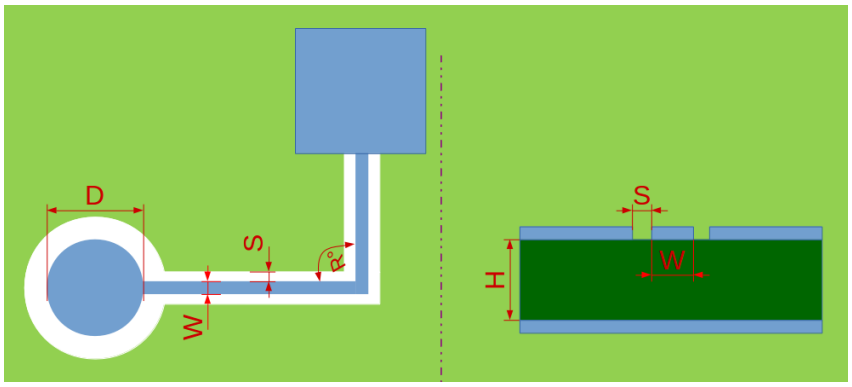

Fig. 18: ESP32-P4 Sensor Track Routing Requirements

Waterproof and Proximity Sensing Design

ESP32-P4 touch sensor has a waterproof design and features proximity sensor function. Figure *ESP32-P4 Waterproof and Proximity Sensing Design* shows an example layout of a waterproof and proximity sensing design.

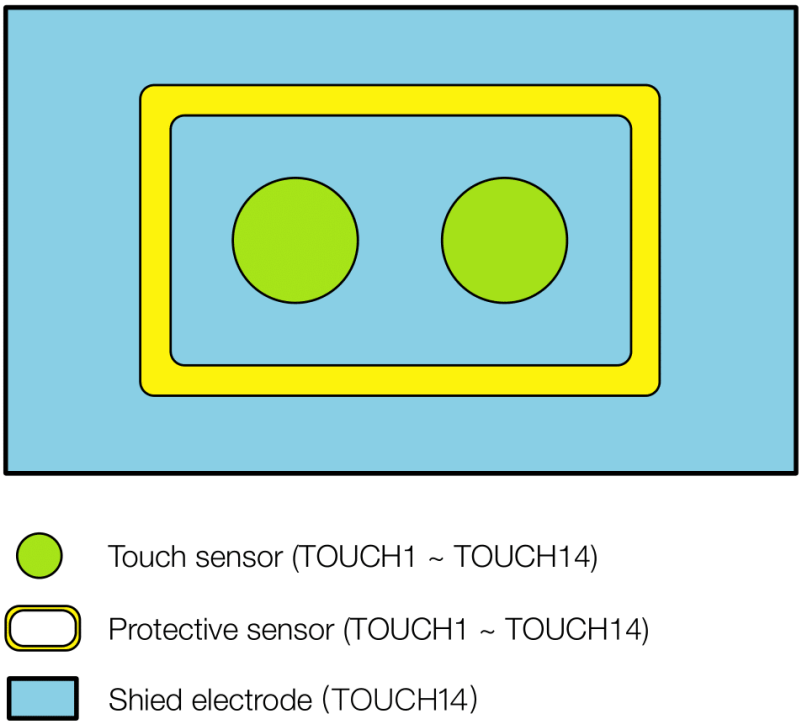

Fig. 19: ESP32-P4 Waterproof and Proximity Sensing Design

Note the following guidelines to better implement the waterproof and proximity sensing design:

- The recommended width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.

- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- The recommended width of the protective sensor is 2 mm.
- The recommended gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce more noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

Note: For more details on the hardware design of the touch sensor, please refer to Touch Sensor Application Note.

1.4.6 MIPI

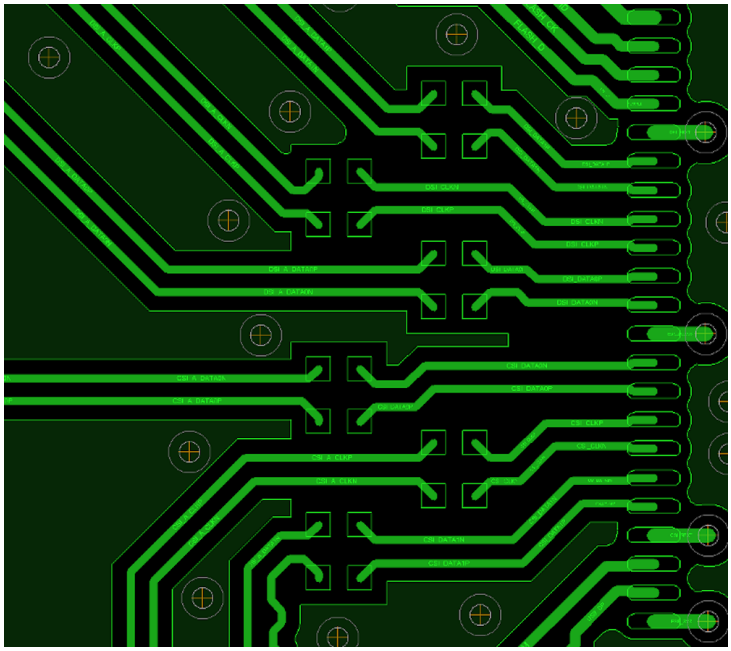

Fig. 20: ESP32-P4 MIPI Layout

The MIPI layout should follow the guidelines below:

- Minimize parasitic capacitance of MIPI traces as they involve high-speed signals.
- The impedance of MIPI differential lines should be controlled to 100 Ω, with a tolerance of ±10%.
- MIPI traces should be kept equal in length and spacing. The length difference between two MIPI traces in a pair should be minimized and kept within 10 mil; the length difference between different MIPI trace pairs should be minimized and kept within 30 mil. Use serpentine routing if necessary.
- It is recommended to surround MIPI trace pairs with ground copper. If this is not feasible, maintain a minimum spacing of 2W between MIPI trace pairs, where "W" is the width of the MIPI trace. For the MIPI CLK trace, surround it with ground copper.
- MIPI signal traces should be kept away from other high-speed and high-frequency signals (such as parallel data traces and clock traces) by at least 3W and must not run parallel to them. They should also be kept away from switching power sources and other sources of interference.
- Ensure there is a continuous reference layer (preferably a ground layer) below the MIPI signal traces.
- For multi-layer PCB designs, it is recommended to route MIPI traces to an inner layer through vias immediately after being drawn out from the chip. This helps minimize interference with high-speed signal lines. Ensure the MIPI CLK traces are surrounded by ground copper. Add a pair of ground return vias at each via transition point.

1.5 Hardware Development

1.5.1 ESP32-P4 Development Boards

This section lists only sample and mass-production ESP32-P4 development boards. For the complete list, see the Development Boards page on the Espressif website.

- ESP32-P4X-C5-Function-EV-Board
- ESP32-P4X-EYE
- ESP32-P4X-Function-EV-Board

1.5.2 Download Guidelines

You can download firmware to ESP32-P4 series chips via UART and USB.

To download via UART:

1. Before the download, make sure to set the chip to Joint Download Boot mode, according to Table *Chip Boot Mode Control*.
2. Power up the chip and check the log via the UART0 serial port. If the log shows "waiting for download", the chip has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using the Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO35 high or leave it floating to make sure that the chip enters SPI Boot mode.
5. Power up the chip again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. If the flash is empty, set the chip to Joint Download Boot mode, according to Table *Chip Boot Mode Control*.
2. Power up the chip and check the log via USB serial port. If the log shows "waiting for download", the chip has entered Joint Download Boot mode.
3. Download your firmware into flash via USB using Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO35 high or leave it floating to make sure that the chip enters SPI Boot mode.
5. Power up the chip again. The chip will read and execute the new firmware during initialization.
6. If the flash is not empty, start directly from Step 3.

Note:

- It is advised to download the firmware only after the "waiting for download" log shows via the serial port.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one COM port.
- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip to Joint Download Boot mode first by configuring the strapping pin.
  - USB PHY is disabled by the application.
  - USB is secondary developed for other USB functions, e.g., USB host, USB standard device.
  - USB IOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.

1.6 Related Documentation and Resources

1.6.1 ESP32-P4 Development Boards

This section lists only sample and mass-production ESP32-P4 development boards. For the complete list, see the Development Boards page on the Espressif website.

- ESP32-P4X-C5-Function-EV-Board
- ESP32-P4X-EYE
- ESP32-P4X-Function-EV-Board

For development board reference designs please refer to:

Note: Use the following tools to open the files in development board reference designs:

- .DSN files: OrCAD Capture V16.6
- .brd files: Allegro 16.6

For the terms applicable to the use of these reference designs, please refer to *Terms of Use for Reference Designs* in *Disclaimer and Copyright Notice*.

1.6.2 Other Related Documentation and Resources

- Chip Datasheet (PDF)
- Technical Reference Manual (PDF)
- Chip Errata
- Consolidated Pin Overview Excel
- ESP32-P4 Chip Variants
- Espressif KiCad Library
- ESP Product Selector
- Regulatory Certificates
- User Forum (Hardware)
- Technical Support
- ESP-FAQ

1.7 Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor acts as a placeholder in the circuit, allowing for the replacement with a higher-ohm resistor based on specific design requirements.

1.8 Revision History

Table 10: Revision History

Date	Version	Release Notes
2026-07-21	v1.9	•***Schematic Checklist*** – Section *Chip Power-up and Reset Timing*: Updated the recommended capacitor value for the CHIP_PU RC delay circuit from 0.1 µF to 1 µF •***PCB Layout Design*** – Section *Power Supply*: Promoted to a top-level section
2026-07-06	v1.8	•***Schematic Checklist*** – Section *Internal Voltage Regulators and External DCDC*: Added two verified DCDC models: BL8028 and LP3219 – Section *USB*: Standardized the peripheral name: USB 2.0 Full-Speed OTG and USB 2.0 High-Speed OTG
2026-06-11	v1.7	•***Schematic Checklist*** – Section *USB PHY Power Supply*: Fixed a typo related to the VDD_USBPHY circuit – Section *Touch Sensor*: Updated descriptions about the touch sensor – Fixed inconsistencies between the English and Chinese versions
2026-04-15	v1.6	•***Schematic Checklist*** – Section *HP/LP IO Power Supply*: Modified the recommended operating voltage for VDD_IO_0, VDD_IO_4, VDD_IO_5, and VDD_IO_6 – Section *Flash and PSRAM IO Power Supply*: Modified the recommended operating voltage for VDD_FLASHIO
2026-02-05	v1.5	*Related Documentation and Resources*: Added the reference design for development boards
2026-02-04	v1.4	•***Schematic Checklist*** – Overview: Added notes on the main differences between chip revisions v1.0/v1.3 (not recommended for new designs) and v3.0 and later versions, and updated the corresponding reference design schematics – Section *Power Supply*: Modified the minimum supply current – Section *USB PHY Power Supply*: Added notes when using DP and DM, and added a reference schematic for VDD_USBPHY – Section *Analog Power Supply*: Modified the operating voltage range of pin VDD_BAT – Section *Internal Voltage Regulators and External DCDC*: Updated notes on VDDO_FLASH output voltage configuration, added notes for circuit layout for different chip revisions, and added the corresponding TLV62569 schematic – Section *SDIO*: Updated SDIO GPIO pin assignment description and fixed a typo in Figure *ESP32-P4 SD 3.0 Card Power Circuit* – Section *USB*: Added instructions for adding a pull-down resistor on the DP pin (applicable to chip revisions v1.0 and v1.3) – Section *Ethernet MAC*: Corrected EMAC signal RMII_RXDV to RMII_CRSDV •***PCB Layout Design*** – Section *Power Supply*: Added recommendation that power traces for pins VDD_BAT and VDD_ANA should be at least 10 mil • *Related Documentation and Resources*: Added Consolidated Pin

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