

乐鑫 ESP32-C5 系列产品升级 Upgrade of ESP32-C5 Series Products			
PCN 编号 PCN No.	PCN20251201	提出日期 Issue Date of PCN	2026/02/27
变更日期 Proposed Date of Change	2026/04/30	预计变更后产品首次 出货日期 Proposed Date of First Shipment After Change	2026/05/30
PCN 类型 PCN Category	<input checked="" type="checkbox"/> 客户需要批准/ Customer Approval Required <input type="checkbox"/> 客户通知/ Customer Notification		
1. 影响物料编码/ Affected Part Number 受影响产品包括 ESP32-C5 系列芯片、模组、开发板，具体物料编码清单如下： The affected products include the ESP32-C5 series chips, modules, and development boards. Part number list is as follows:			
1) 芯片产品/ Chip Products			
物料编码 Part Number		变更项目 Change Item	
ESP32-C5HR8		Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.	
ESP32-C5HF4		a) Upgraded the ESP32-C5 chip revision from v1.0 to v1.2. b) Updated the ESP32-C5HF4 pin layout.	
2) 模组产品/ Module Products			
模组名称 Module Product Name	物料编码 Part Number	内置乐鑫芯片 Chip on Board	变更项目 Change Item
ESP32-C5-MINI-1	ESP32-C5-MINI-1-N4	ESP32-C5HF4	a) Upgraded the ESP32-C5 chip revision from v1.0 to v1.2. b) Updated the ESP32-C5HF4 pin layout. c) Updated the module schematics to align with the ESP32-C5HF4 pin layout changes.
ESP32-C5-WROOM-1	ESP32-C5-WROOM-1-N4	ESP32-C5HF4	a) Upgraded the ESP32-C5 chip revision from v1.0 to v1.2. b) Updated the ESP32-C5HF4 pin layout. c) Updated the module schematics to align with the ESP32-C5HF4 pin layout changes.
ESP32-C5-WROOM-1U	ESP32-C5-WROOM-1U-N4	ESP32-C5HF4	a) Upgraded the ESP32-C5 chip revision from v1.0 to v1.2. b) ESP32-C5HF4 Pin Layout updates c) Updated the module schematics to align with the ESP32-C5HF4 pin layout changes.
ESP32-C5-WROOM-1	ESP32-C5-WROOM-1-N8R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.
ESP32-C5-WROOM-1	ESP32-C5-WROOM-1-N16R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.
ESP32-C5-WROOM-1	ESP32-C5-WROOM-1-N32R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.
ESP32-C5-WROOM-1U	ESP32-C5-WROOM-1U-N8R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.

ESP32-C5-WROOM-1U	ESP32-C5-WROOM-1U-N16R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.
ESP32-C5-WROOM-1U	ESP32-C5-WROOM-1U-N8R8T2	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.
ESP32-C5-WROOM-1U	ESP32-C5-WROOM-1U-N16R8T2	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.

3) 开发板产品/ Development Board Products

产品名称 Product Name	物料编码 Part Number	内置乐鑫芯片 Chip on Board	变更项目 Change Item
ESP32-C5-DevKitC-1	ESP32-C5-DevKitC-1-N8R8	ESP32-C5HR8	Upgraded the ESP32-C5 chip revision from v1.0 to v1.2.

2. 变更原因/ Reason for Change

乐鑫 ESP32-C5 系列产品持续升级优化。

The ESP32-C5 series continues to be enhanced and optimized.

3. 变更描述/ Description of Change

1) ESP32-C5 系列产品的芯片硬件金属层变更，芯片版本由 v1.0 升级为 v1.2。

- 更新了 ROM 代码，在检测到 HUK 恢复失败的情况下重新给 HUK 上电，确保所有环境下（电压不稳、高低温等）HUK 能够正确恢复，保证后续密钥的恢复顺利完成；
- 更新了 ROM 代码，将部分 Wi-Fi 和 PHY 相关的函数固化在 ESP32-C5 芯片版本 v1.2 的 ROM 中，节省了 ESP32-C5 芯片版本 v1.2 中 SRAM 和 flash 内存空间的占用；
- 解决了 PSRAM 先写后读一致性问题；
- 修复了因数字外设电源域掉电导致 SRAM 内容被改写问题，支持 Light-sleep 模式配置数字外设电源域掉电，从而降低了 Light-sleep 模式下的睡眠电流。

ESP32-C5 芯片版本 v1.2 优化信息参见[附录 I-2](#)。

2) ESP32-C5HF4 系列产品管脚定义更新。

- ESP32-C5HF4 芯片：
芯片管脚定义更新，其内置 SiP flash 与主芯片的连接不再通过芯片引脚连接，而是直接在封装内部互联，从物理上隔断了外部操作合封 flash 的可能性；芯片技术规格书更新；
- 基于 ESP32-C5HF4 芯片的模组：
模组内 flash 相关的器件去除；模组原理图更新；模组技术规格书更新。

ESP32-C5HF4 系列产品管脚定义更新信息参见[附录 I-3](#)。

1) The ESP32-C5 series chips have undergone a wafer metal change, and the chip revision has been upgraded from v1.0 to v1.2.

- The ROM code has been updated to re-power the HUK and retry recovery when a HUK recovery failure is detected, ensuring reliable HUK recovery under all operating

conditions (such as unstable voltage and high/low temperatures) and guaranteeing successful recovery of subsequent keys.

- The ROM code has been updated to move some Wi-Fi- and PHY-related functions into the ROM of ESP32-C5 chip revision v1.2, thereby reducing SRAM and flash memory usage on ESP32-C5 v1.2 chips.
- The PSRAM write-before-read consistency issue has been resolved.
- The issue where SRAM contents could be corrupted due to digital peripheral power domain power-down has been fixed. Digital peripheral power domain power-down is now supported in light-sleep mode, reducing sleep current consumption during light-sleep.

Optimization details for ESP32-C5 chip revision v1.2 are provided in [Appendix I-2](#).

2) The ESP32-C5HF4 products have updated pin definitions.

- For the ESP32-C5HF4 chip, the pin definitions have been updated in the chip datasheet. The internal SiP flash is no longer connected to the main chip through external pins; instead, it is directly interconnected within the package. This physically prevents external access to, or operations on, the in-package flash.
- For modules based on ESP32-C5HF4, flash-related components have been removed. The schematics for the modules have been revised accordingly in the module datasheets.

Pin definitions update information of the ESP32-C5HF4 products is provided in [Appendix I-3](#).

4. 变更对比/ Change Comparison

请见附录 I：变更对比。

Please refer to Appendix I: Change Comparison.

识别方式/ Identification Method:

芯片产品：通过产品 eFuse 及产品丝印。

模组和开发板产品：通过主芯片的 eFuse，模组屏蔽盖丝印的产品规格标识位，或产品外箱标签中的 PW 号。

Chips: Identified by the eFuse bits and the chip marking.

Modules and development boards: Identified by the chip's eFuse bits, the specification identifier on the module shield-cover marking, or the PW number on the product outer-box label.

5. 变更影响/ Impact of Change

1) 品质和性能/ Quality & Performance:

- a) ESP32-C5 芯片版本 v1.2 优化信息参见[附录 I-2](#)。
- ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用，可使用 ROM 中基于 HUK 的 flash 加解密密钥部署，ESP-IDF 中的 HUK 功能；
 - ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用，可以额外获得约 6 KB SRAM 空间和约 20 KB flash 内存空间；
 - ESP32-C5 芯片版本 v1.2 解决了因 PSRAM 先写后读一致性问题导致的 PSRAM 加解密异常等问题；
 - ESP32-C5 芯片版本 v1.2 解决了因数字外设电源域掉电导致 SRAM 内容被改写问题。ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用，可以配置 Light-sleep 模式下数字外设电源域掉电从而降低了约 100 μ A 的睡眠电流。
- b) ESP32-C5HF4 产品的管脚定义更新和 ESP32-C5HF4 系列模组原理图更新对产品品质和性能无影响，提高产品的安全性能。客户使用变更后的 ESP32-C5HF4 系列芯片和模组，请参照最新的技术规格书。如需对 ESP32-C5HF4 进行 SPI 烧录器烧录，请联系[乐鑫](#)确认。
- a) Optimization details for ESP32-C5 chip revision v1.2 are provided in [Appendix I-2](#).
- When used with an upgraded ESP-IDF, ESP32-C5 chip revision v1.2 supports deployment of HUK-based flash encryption/decryption keys from ROM, as well as HUK functionality provided by ESP-IDF.
 - When used with an upgraded ESP-IDF, ESP32-C5 chip revision v1.2 provides approximately 6 KB of additional SRAM space and approximately 20 KB of additional flash memory space.
 - ESP32-C5 chip revision v1.2 resolves PSRAM encryption/decryption exceptions caused by the PSRAM write-before-read consistency issue.
 - ESP32-C5 chip revision v1.2 fixes the issue where SRAM contents could be corrupted due to digital peripheral power domain power-down. When used with an upgraded ESP-IDF, digital peripheral power domain power-down can be enabled in light-sleep mode, reducing sleep current by approximately 100 μ A.
- b) The updates to the pin definitions of the ESP32-C5HF4 product and the schematic revisions for ESP32-C5HF4 series modules have no impact on product quality or performance and instead enhance product security. Customers using the updated ESP32-C5HF4 chips and modules should refer to the latest datasheets. If SPI programming is required for ESP32-C5HF4, please [contact us](#).

2) 交期/ Delivery: 无影响/ No impact

3) 物料编码/ Part Number: 无影响/ No impact

4) 软件/ Software:

- a) ESP32-C5 芯片版本 v1.2 系列产品搭载现有 ESP-IDF 版本，产品可正常使用。
- b) ESP32-C5 芯片版本 v1.2 部分优化，需搭载升级后的 ESP-IDF 版本实现。具体信息如下：

i) 根据下表升级 ESP-IDF 版本：

ESP-IDF Branch	Required ESP-IDF Version	Recommended ESP-IDF Version
release/v6.0	v6.0	v6.0+
release/v5.5	<ul style="list-style-type: none"> • HUK feature: v5.5.2 • Access the additional SRAM and flash memory space: v5.5.3 • Power Down Digital Peripheral in Light-sleep Mode: v5.5.3 	v5.5.3+

ii) 如使用芯片版本 v1.2 的数字外设电源域掉电功能时，会节省约 100 μ A 的睡眠电流。需执行 i) 及下述配置：

运行 ESP-IDF 的工程配置工具“menuconfig”，将“Power down Digital Peripheral in light sleep”(> Component config > Power Management) 设置为“y”。默认值是“n”。使用该配置请参考[说明文档](#)。

```
(Top) → Component config → Power Management
Espressif IoT Development Framework Configuration
+*- Place Power Management module functions in IRAM
[*] Support for power management
  [ ] Enable dynamic frequency scaling (DFS) at startup
  [ ] Enable profiling counters for PM locks
  [ ] Enable debug tracing of PM using GPIOs
+*- Put lightsleep related codes in internal RAM
+*- Put RTOS IDLE related codes in internal RAM
+*- Disable all GPIO when chip at sleep
(1) Calibrate the RTC_FAST/SLOW clock every N times of light sleep
[*] Power down CPU in light sleep
  [ ] Power down Digital Peripheral in light sleep (EXPERIMENTAL)
  [ ] Enable registration of pm light sleep callbacks
```

其他情况下(如使用 ESP32-C5 芯片版本 v1.0 及之前芯片版本或维持“Power down Digital Peripheral in light sleep”选项为默认值“n”)，产品 Light-sleep 睡眠功能正常，但不会带来 100 μ A 的睡眠电流优化。

iii) 如使用芯片版本 v1.2 的 HUK 功能或(和)额外获得约 6 KB SRAM 和 20 KB flash 空间时，需执行 i)， “menuconfig” 中需配置 “Minimum Supported ESP32-C5 Revision”：

运行 ESP-IDF 的工程配置工具“menuconfig”时，将“Minimum Supported ESP32-C5 Revision”(> Component config > Hardware Settings > Chip revision) 设置为“Rev v1.2”。默认值是“Rev v1.0”。



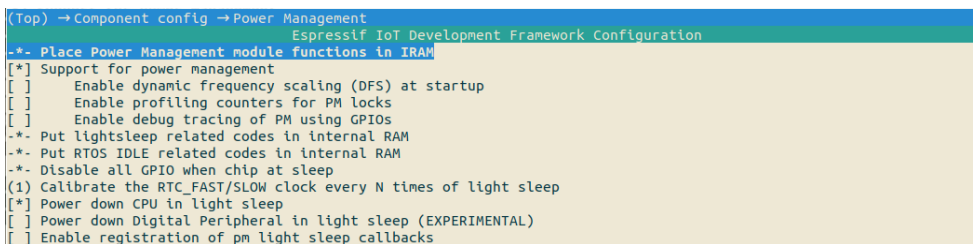
注意：若将“Minimum Supported ESP32-C5 Revision”配置为“Rev v1.2”时，固件无法兼容 ESP32-C5 芯片版本 v1.0 及之前芯片版本。

- a) ESP32-C5 chip revision v1.2 series products can operate normally with existing ESP-IDF versions.
- b) Some optimizations introduced in chip revision v1.2 require an updated ESP-IDF version.
 - i) Upgrade the ESP-IDF version according to the table below:

ESP-IDF Branch	Required ESP-IDF Version	Recommended ESP-IDF Version
release/v6.0	v6.0	v6.0+
release/v5.5	<ul style="list-style-type: none"> • HUK feature: v5.5.2 • Access the additional SRAM and flash memory space: v5.5.3 • Power Down Digital Peripheral in Light-sleep Mode: v5.5.3 	v5.5.3+

- ii) When using the digital peripheral power domain power-down feature on chip revision v1.2, approximately 100 μ A of sleep current can be saved. Item (i) and the following configuration must be applied:

Run the ESP-IDF project configuration tool menuconfig, and set “Power down Digital Peripheral in light sleep” (> Component config > Power Management) to “y”. The default value is “n”. Please refer to the [documentation](#) for details on using this configuration.

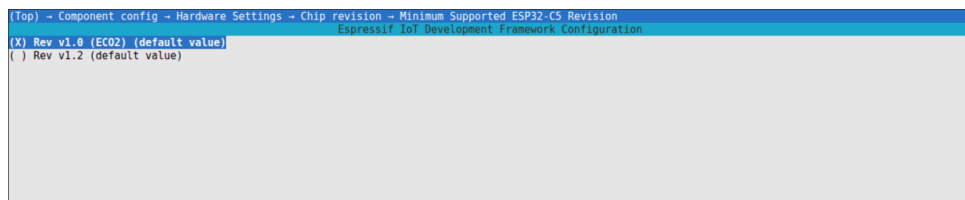


In other cases (for example, when using ESP32-C5 chip revision v1.0 or earlier, or when leaving the “Power down Digital Peripheral in light sleep” option at its default value of “n”), the product’s light-sleep mode operates normally, but no $\sim 100 \mu$ A reduction in sleep current is achieved.

- iii) If you intend to use the HUK-based features, or to use the additional 6 KB SRAM and 20 KB flash memory available in chip revision v1.2, please follow item (i) and set

“Minimum Supported ESP32-C5 Revision” in “menuconfig”:

Run the ESP-IDF project configuration tool menuconfig, and set “Minimum Supported ESP32-C5 Revision” (> Component config > Hardware Settings > Chip revision) to “Rev v1.2”. The default value is “Rev v1.0”.



Note: If the “Minimum Supported ESP32-C5 Revision” is set to “Rev v1.2”, the firmware will be incompatible with ESP32-C5 chip revisions v1.0 and earlier.

5) 认证/ Certification: 无影响/ No impact

6) 技术规格书/ Datasheet:

[ESP32-C5 系列芯片技术规格书/ ESP32-C5 Series Datasheet](#)

[ESP32-C5-MINI-1 技术规格书/ ESP32-C5-MINI-1 Datasheet](#)

[ESP32-C5-WROOM-1 & ESP32-C5-WROOM-1U 技术规格书/ ESP32-C5-WROOM-1 & ESP32-C5-WROOM-1U Datasheet](#)

[ESP32-C5 系列芯片勘误表/ ESP32-C5 Series SoC Errata](#)

6. 变更前后产品处理/ How to Deal with Products

FIFO

7. 相关报告/ Related Report(s)

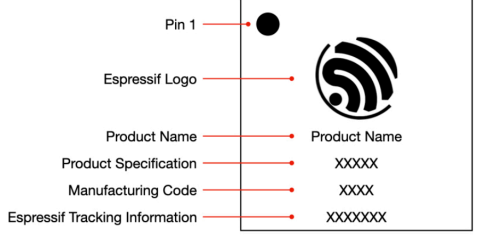
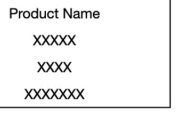
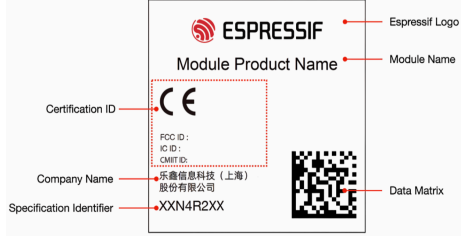
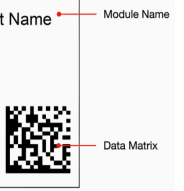
RF Performance Test Report Pass

8. 给使用者的验证建议/ Verification Suggestion to Users

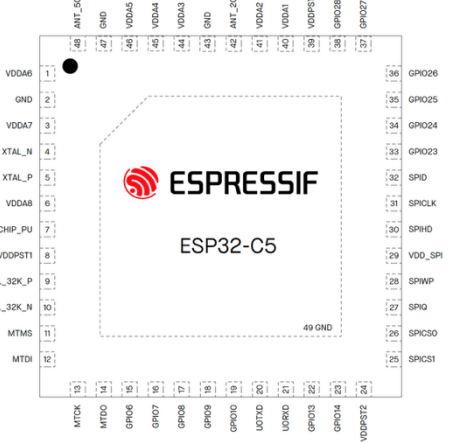
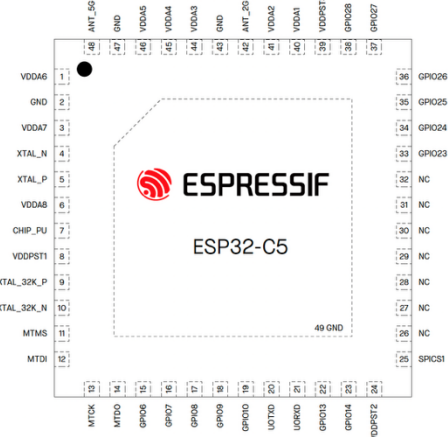
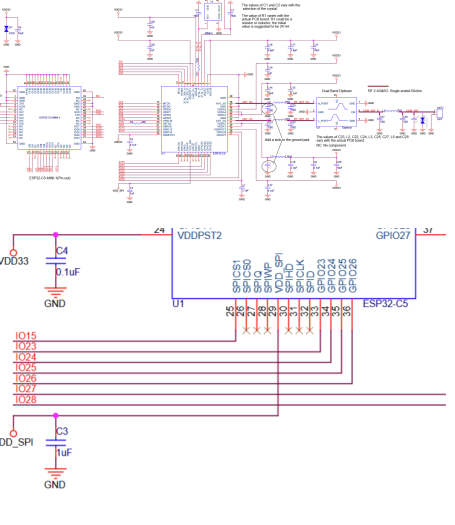
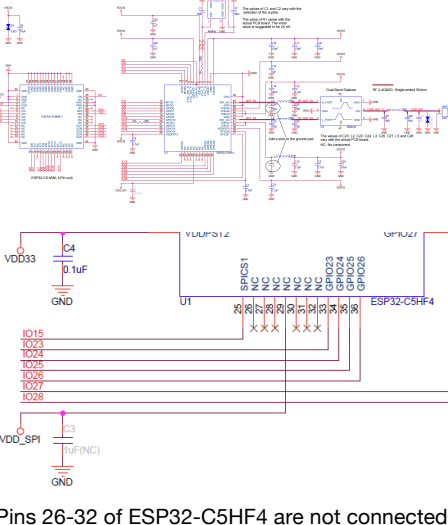
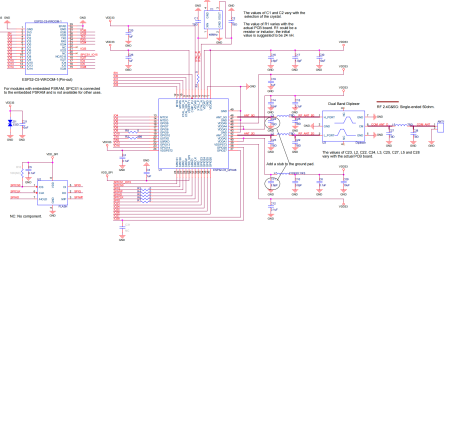
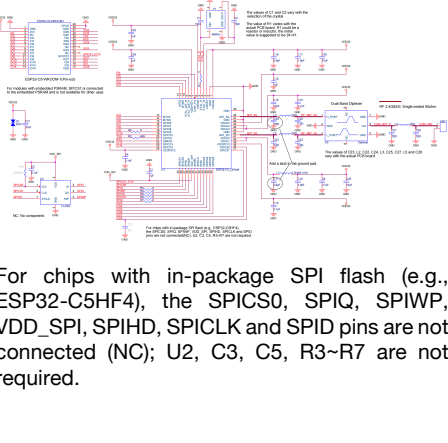
建议客户升级 ESP-IDF 至最新稳定版本，截止文档发布时，ESP-IDF 最新稳定版本是 ESP-IDF v5.5.3。

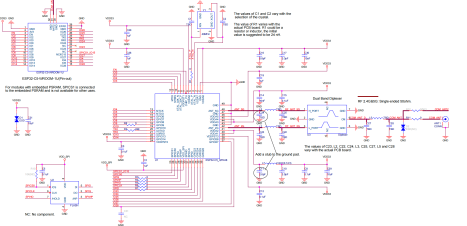
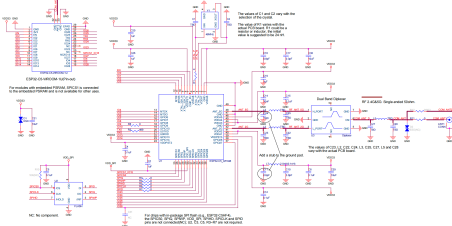
It is recommended that customers use the latest stable ESP-IDF release. As of the publication date of this PCN, the latest stable version is ESP-IDF v5.5.3.

Appendix I 变更对比/ Change Comparison

1 产品基本信息/ Product Basic Information				
No.	项目/ Item		变更前/ Before Change	变更后/ After Change
1.1	ESP32-C5 Chip Revision		v1.0	v1.2
1.2	ESP32-C5 芯片版本 eFuse 标识位/ eFuse Identification Bits of ESP32-C5 Chip Revision			
	Wafer_version_Major	EFUSE_RD_MAC_SYS2_REG[5]	0	0
		EFUSE_RD_MAC_SYS2_REG[4]	1	1
	Wafer_version_Minor	EFUSE_RD_MAC_SYS2_REG[3]	0	0
		EFUSE_RD_MAC_SYS2_REG[2]	0	0
		EFUSE_RD_MAC_SYS2_REG[1]	0	1
		EFUSE_RD_MAC_SYS2_REG[0]	0	0
1.3	ESP32-C5 Series Chip Marking (Manufacturing Code Line)			
			xCXX	xDXX
1.4	ESP32-C5 Series Module Marking (Specification Identifier Line)			
			MCXXXX	MDXXXX

2 ESP32-C5 优化信息/ Optimization of ESP32-C5			
No.	项目/ Item	变更前/ Before Change	变更后/ After Change
2.1	HUK 功能 HUK Feature	HUK 功能不可用 HUK Is Unavailable	修复 HUK 功能, ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用, 可使用 ROM 中基于 HUK 的 flash 加密密钥部署以及 ESP-IDF 中的 HUK 功能, 参见 ESP32-C5 系列芯片技术规格 > 密钥管理器章节 HUK has been fixed. When ESP32-C5 chip revision v1.2 is used with an upgraded ESP-IDF, it supports deployment of HUK-based flash encryption keys from ROM, as well as HUK functionality provided by ESP-IDF. Refer to ESP32-C5 Series Datasheet > Section Key Manager.
2.2	ESP32-C5 SRAM 和 flash 内存空间 ESP32-C5 SRAM and Flash Memory	正常使用 Normal Usage	ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用, 可以额外获得约 6 KB SRAM 空间, 额外获得约 20 KB flash 内存空间。 Using ESP32-C5 chip revision v1.2 with the upgraded ESP-IDF provides approximately 6 KB of additional SRAM and 20 KB of additional flash memory.
2.3	PSRAM 加解密 PSRAM Encryption/Decryption	出现因 PSRAM 先写后读一致性问题导致 PSRAM 加解密异常 Encryption/Decryption exceptions caused by the PSRAM write-before-read consistency issue	已修复 Fixed
2.4	SRAM	1. 出现因数字外设电源域掉电导致内部 SRAM 内容被改写问题。 2. 不支持 Light-sleep 模式配置数字外设电源域掉电功能。 1. Internal SRAM contents may be corrupted when the digital peripheral power domain is powered down. 2. The digital peripheral power domain power-down feature is not supported in light-sleep mode.	1. ESP32-C5 芯片版本 v1.2 已修复因数字外设电源域掉电导致内部 SRAM 内容被改写问题。 2. ESP32-C5 芯片版本 v1.2 与升级后的 ESP-IDF 搭载使用, 可以配置 Light-sleep 模式下数字外设电源域掉电从而降低约 100 μ A 的睡眠电流, 使用该功能参见 说明文档 。 1. In ESP32-C5 chip revision v1.2, the issue where internal SRAM contents could be corrupted due to digital peripheral power domain power-down has been fixed. 2. When ESP32-C5 chip revision v1.2 is used with an upgraded ESP-IDF, the digital peripheral power domain power-down feature can be enabled in light-sleep mode, reducing sleep current by approximately 100 μ A. Please refer to the documentation for instructions on using this feature.
2.5	其他优化请参见 ESP32-C5 系列芯片勘误表 For additional optimizations, please refer to the ESP32-C5 Series SoC Errata .		

3	ESP32-C5HF4 系列产品管脚定义更新信息/ Pin Definitions Update Information of the ESP32-C5HF4 Products		
No	项目/ Item	变更前/ Before Change	变更后/ After Change
3.1	ESP32-C5 Series Datasheet (ESP32-C5HF4 Pin Layout)		 <p>Pins 26-32 are not connected (NC).</p>
3.2	ESP32-C5-MINI-1 Datasheet (ESP32-C5-MINI-1 Schematics)		 <p>Pins 26-32 of ESP32-C5HF4 are not connected (NC); C3 of module is not required.</p>
3.3	ESP32-C5-WROOM-1 & ESP32-C5-WROOM-1U Datasheet (ESP32-C5-WROOM-1 Schematics)		 <p>For chips with in-package SPI flash (e.g., ESP32-C5HF4), the SPICS0, SPIQ, SPIWP, VDD_SPI, SPIHD, SPICLK and SPID pins are not connected (NC); U2, C3, C5, R3~R7 are not required.</p>

No	项目/ Item	变更前/ Before Change	变更后/ After Change
3.4	ESP32-C5-WROOM-1 & ESP32-C5-WROOM-1U Datasheet (ESP32-C5-WROOM-1U Schematics)		 <p>For chips with in-package SPI flash (e.g., ESP32-C5HF4), the SPICS0, SPIQ, SPIWP, VDD_SPI, SPIHD, SPICLK and SPID pins are not connected (NC); U2, C3, C5, R3~R7 are not required.</p>

邮件订阅
Espressif Email Notifications

乐鑫为注册用户提供电子邮件通知服务，用户可通过[乐鑫订阅系统](#)接收技术文档更新、新闻通讯、PCN 等邮件通知。

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客户响应要求
Customer Response Requirements
需客户批准的变更/ Change Requiring Customer Approval:

- a) 客户须在乐鑫发出 PCN 后的 30 天内告知乐鑫已收到 PCN。如客户未在接收到 PCN 后的 30 天内告知已收到，则视为客户收到变更。

Customers are requested to acknowledge receipt of the PCN within 30 calendar days from the date of issue of the PCN. Customers would be considered as notified 30 calendar days after issue of the PCN if no acknowledgement is received.

- b) 自发布 PCN 之日起 90 天内，客户没有任何其他反馈，则表示客户接受该 PCN。

The lack of any additional responses from customers within 90 calendar days from the date of issue of the PCN constitutes acceptance of the proposed changes.

客户通知/ Customer Notification:

- a) 客户需在乐鑫发出 PCN 后 14 天内通知乐鑫收到该 PCN。如客户未在接收到 PCN 14 日反馈乐鑫，则视为客户确认该 PCN。

Customers are requested to acknowledge receipt of the PCN within 14 calendar days from the date of issue of the PCN. Customers would be considered as having acknowledged the PCN if no response is received after 14 calendar days.

请反馈至 pcn@espressif.com。

Please send feedback to pcn@espressif.com.

客户批准/确认信息
Customer Approval / Acknowledgement and Remarks

客户公司全称:

Customer's Company Name:

PCN 评审结果
PCN Review Result

- 批准/确认 Accepted / Acknowledged
 不批准 Rejected
 需要分析 Further Analysis Required

客户意见/ Comment:

公司代表人姓名
Representative's Name

公司代表人职责
Representative's Job Title

公司代表人签名
Representative's Signature

日期
Date