Compatibility Advisory

Title	Compatibility Advisory for ESP32-P4 Chip Revision v3.2
Issue Date	2026/05/15
Advisory Number	AR2026-004
Serial Number	NA
Version	V1.0

Introduction

We have upgraded the ESP32-P4 chip to revision v3.2. The latest chip revision fixes several known hardware issues present in earlier versions. For details, please refer to the ESP32-P4 Series SoC Errata.

The hardware of different sub-revisions within ESP32-P4 v3.x is fully compatible. The following mainly evaluates software compatibility.

1. **Esptool Flashing Tool Incompatibility**

   The esptool must be updated to at least version v5.3.dev3 (for v6.0 and later) or v4.12.dev2 (for v5.5.3 and later) to support the ROM feature in v3.2 chips that automatically powers on the flash, enabling normal firmware downloading. After using the corresponding version of ESP-IDF and re-running install, esptool will be upgraded automatically.

2. **wdt_hal_config_stage API Incompatibility**

   In ESP32-P4 chip revision v3.1 and earlier, an issue exists in the RTC watchdog configuration API provided by ROM: the hardware watchdog timeout is twice the configured software value. In ESP-IDF, this API is wrapped with a workaround by adjusting the timeout tick value passed to ROM, ensuring the actual timeout matches the configured value.

   Starting from **ESP32-P4 chip revision v3.2**, this issue has been fixed in the chip ROM. The hardware timeout now matches the software configuration, and the above software compensation is no longer needed.

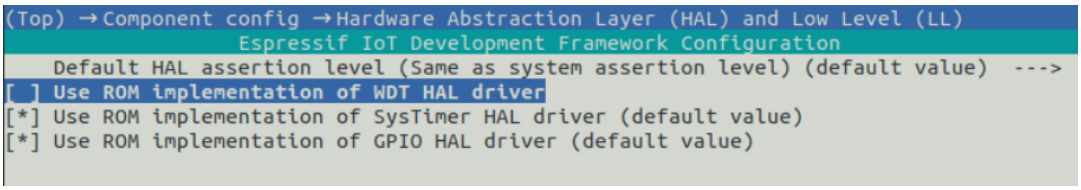
   However, in some ESP-IDF versions, the wrapper logic does not read eFuse to distinguish chip revisions and instead applies the compensation intended for v3.1 and earlier ROM to all chip revisions. When such firmware runs on v3.2 and later chips, the compensation is applied twice, causing the hardware timeout to be approximately half of the configured value.

Impact: If the slow clock is configured as external 32 kHz crystal in menuconfig, but no external 32 kHz crystal is present on the hardware, or the crystal fails to oscillate due to external factors even though it is populated, the slow clock detection during startup may take longer than expected. As a result, the LP watchdog timer (LP_WDT) timeout period may become insufficient, causing repeated LP_WDT resets during the boot process.

Required ESP-IDF Version for Using an External 32 kHz Crystal with ESP32-P4 Chip Revision v3.2

Release Branch	Recommended Version	Minimum Required Version
master	/	v6.1
release/v6.0	v6.0.1+	v6.0.1
release/v5.5	v5.5.5+	v5.5.5

1. It is recommended to upgrade ESP-IDF to the versions listed in the table above.
2. If upgrading ESP-IDF is not feasible in the short term, you can mitigate the risks described in this notice by disabling **CONFIG_HAL_WDT_USE_ROM_IMPL** in menuconfig (this will increase internal RAM usage by approximately 1 KB).



Chip Revision Identification

For information on how to identify the chip revision, please refer to ESP32-P4 Chip Revision Identification.

For additional explanations on software compatibility, please refer to Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.

Contact

If you need technical assistance, please contact Espressif.